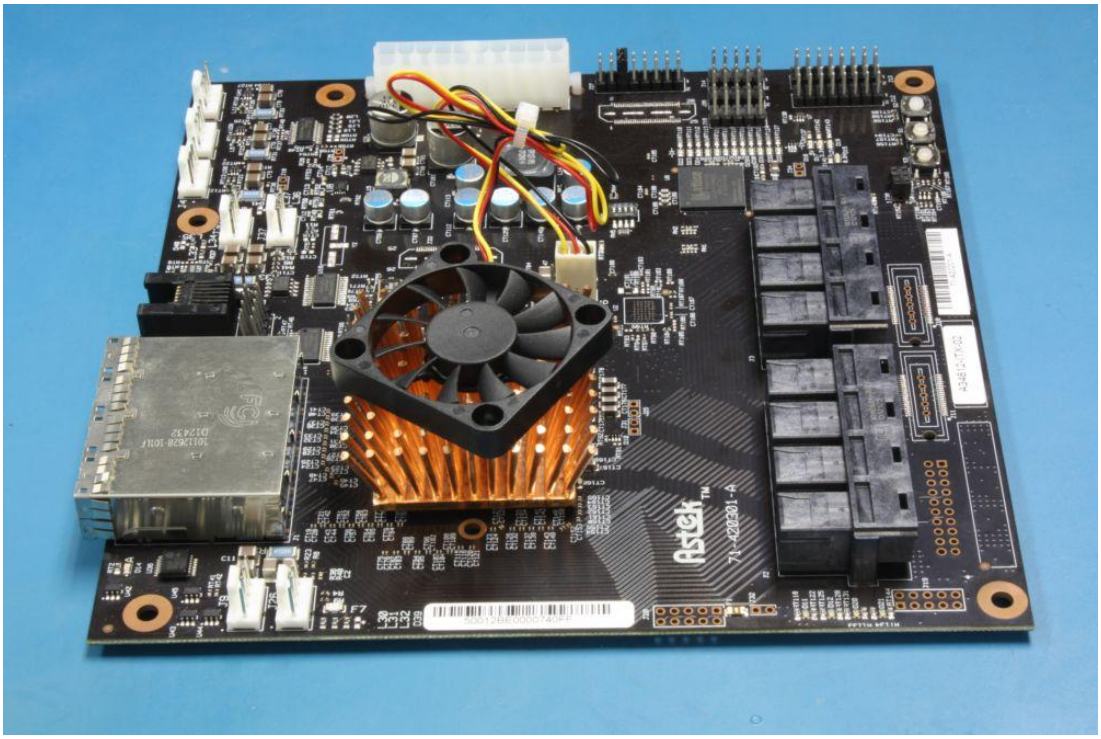

# A34812-ITX

## User's Manual

**July, 2016**

This document describes Astek's A34812-ITX "Mogul" design and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

To receive product literature, visit us at http://www.astekcorp.com.

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Note: The A34812-ITX has been designed to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These Limits are designed to provide reasonable protection against harmful interference when the equipment is operated in its installation. This equipment generates, uses, can radiate radio frequency energy, and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. If this equipment does cause harmful interference the user will be required to correct the interference.

The A34812-ITX has been designed to meet the safety requirements of IEC/EN 60950-1.

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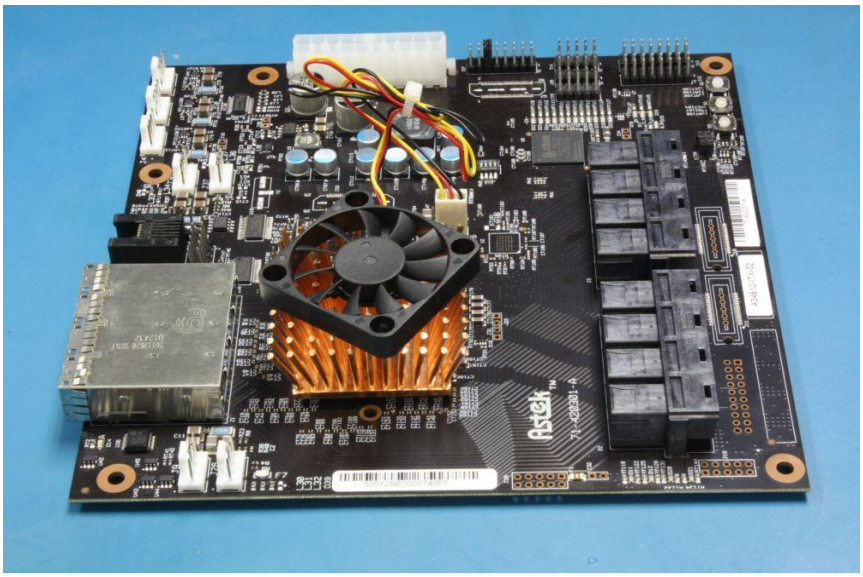
Table of Contents

# 1 Introduction

The Astek A34812-ITX ("Mogul") board is based on the LSI Corporation SAS 3x48 Serial Attached SCSI (SAS) Bus Expander ASIC, and provides up to 48 lanes of 12Gb/s SAS complaint with the SAS r3.0 specification. The board uses a convenient Mini-ITX "PC motherboard" form factor which is compatible with thousands of standard enterprise computing and storage server computer enclosures, and uses a standard TFX12V type power supply. It operates as an appliance, with no management required, and supports on-board firmware applications for advanced systems operation and remote management (requires NRE development by licensed providers including Astek, licenses provided by LSI Corporation to qualified entities).

The board can be used standalone for "Just a Bunch of Disks" (JBOD) enclosures, or as a companion with a host processor board and SAS controller or Host Bus Adapter card. When used standalone, the A34812-ITX supplies a complete set of basic enclosure features such as cooling fan power (with optional sense/control), thermal sensor for environmental control, and both discrete direct driven LED indicators and Serial GPIO (SGPIO) conforming to SFF-8485 for panel indicators with support for individual indicators for every PHY on the expander (physical and virtual).

**Illustration 1: A34812-ITX-02 Board**



## Part Number and Variants

The following ordering part numbers are available for ordering as of the date of this User's Manual:

| Part Number | Variant Information |
|---|---|
| A34812-ITX-02 | 48-ports LSISAS3x48 device |
| | |

# LSISAS3x48 Expander

The expander design incorporates the following features and attributes:

## High Level Features

- 48 phy SAS Expander
  - Fully symmetric phys functionality
    - Any phy  can be combined into wide port(s)
    - Any phy can be SAS or SATA affiliation
    - Ability to disable all SATA affiliations
    - Powered down phys capable of detecting connectivity changes
    - All phys support optical links between SAS-3 devices
  - Supported phy rates
    - 3Gb/s, 6Gb/s, and 12Gb/s SAS
    - 3Gb/s, and 6Gb/s SATA
    - All data rates auto-negotiation on all PHYs
    - Supports spread spectrum modulation
    - *NOTE: 1.Gbps data rates are NOT supported*
  - Drive Spin-up Sequencing Control
    - SAS drives through NOTIFY(ENABLE SPINUP) primitive
    - SATA drives through SATA_DelaySpin Phy state
    - Programmable spin-up sequencing with hot-plug priority
    - Provides configurable drive spin-up sequencing on a per-phy basis
  - Supports multiple routing methodologies
    - Direct, table, subtractive, and dual subtractive (Reverse Table) routing methods
    - Routing method individually configurable per phy
    - N number of routing table entries per phy (total 2048 entries)
    - Allows flexible allocation of routing table entries to the expander phys
    - Does not limit the number of phys composing a wide-port
    - Allows reuse of routing table resources across all of the phys composing a wide-port
  - Supports multiple zoning methods
    - T-10 compliant
    - SASx36 (SAS-1), SAS2x36 (SAS-2) backward compatible phy based zoning
  - Three identical virtual phys supporting SMP, SSP, and STP protocols at up to 12Gb/s with independent Tx and Rx buffers. (These are referred to as Internal SxP ports)
    - SMP Initiator/Target
    - SSP Initiator/Target supporting 4 Tx and Rx buffers. (Up to 4 initial credits on open)
    - STP Initiator
    - Direct Attach Override mode allows multiple CAM entries to map multiple WWN addresses to each of these ports
- 300 MHz Cortex-R4 processor
  - ARM acts as an application layer for SMP port(s) and SxP port(s) for the following optional uses:
    - Small Computer System Interface Enclosure Services (SES)
    - Drive management
    - Self configuration and zoning management
    - Other SMP functions

- Offers an advanced LED and GPIO interface that provide serial and parallel GPIO capabilities
  - 51 I/Os for Link Status LEDs or GPIO
  - 16 GPIOs
  - SFF-8485 compatible SIO (SGPIO)
- Debug/Management capability
  - Generic serial UART
  - 10/100/1000 Ethernet I/F for remote management
  - Port mirroring Phy pair(s) allow non intrusive snooping of any other phy's data stream
  - USB 2.0 device
- Authentication and security support
  - 256-bit SHA accelerator (SHA FIPS-180-2)
  - Keyed-hash message authentication code (HMAC-FIPS 198)
  - 256-bit True random number generator (TRNG)
- Statistical logging counters
  - Selectable (4 of N) subset of T-10 counter requirements for counting various events

- Supports the SAS protocol described in the Serial Attached SCSI (SAS) Standard, version 2.0
- Supports SATA, as defined in the Serial ATA: High Speed Serialized AT Attachment Specification, version 3.0
- Supports SATA II including the following features:
  - 6Gb/s SATA
  - Staggered/programmable spin-up
  - Hot Plug
  - Native Command Queuing
  - Activity and fault indicators per phy
  - Port Selector (for dual port drives)
- Provides a low-latency connection router to efficiently create and maintain connections

## STP Initiator Features

- Supports STP data transfers of up to 12Gb/s
- Supports STP initiator functions using the Cortex-R4 processor or an external processor
- Enables user-customized STP initiator functions, such as drive management:
  - Permits drive queries to qualify drives that are compatible with the system
  - Provides an application layer that enables the implementation of vendor-unique commands

## SMP Initiator and Target Features

- Supports SMP data transfers of up to 12Gb/s
- Supports SMP initiator and target functions using the ARM Cortex-R4 processor
- Provides an SMP initiator that can be used to support operations such as self-discovery and self-configuration
- Provides an SMP target that can implement SMP functions defined in the SAS standard:
  - Uses the SMP Report Manufacturer Information frame format as defined in revision 14 of the SAS-2 Specification
  - Decodes SMP frames that are destined for the expander
- Implements standard SMP features in the firmware using the ARM Cortex-R4 internal RAM
- Enables the implementation of vendor-unique SMP commands with the internal Cortex-R4 processor

## Testing and Reliability Features

- Uses proven SerDes transceivers
- Provides (electrostatic discharge (ESD) protection
- Provides latch-up protection
- Has a high proportion of power and ground pins

- Uses the LSI G40 technology
- Offers a debugging interface through a serial interface
- Supports JTAG testing
- Provides an ARM Multi-ICE® interface for debugging the ARM processor
- Includes the required logic for ATPG SCAN, IDD testing, and Procomon in the Clock/Reset/Misc/JTAG block

### Port Mirroring

- Port Mirroring feature allows the transmit and receive data of one phy to be transmitted on two other phys. This feature is useful when there is a link that has no access to the outside world such as one on a midplane.
- Transmits received data on one phy
- Transmits transmitted data on another phy
- Allows snooping of a link

# 2 Installation Procedures

## Hardware Installation

| | |
|---|---|
| **CAUTION** | Use proper ESD safety procedures whenever working with electronic equipment or parts. |

Step 1. Remove the A34812-ITX from the ESD packaging and check that it is not damaged.

Step 2. Secure the card in the enclosure using the four (4) mini-ITX compliant mounting holes.

Step 3. Attach a 20-pin power cable from the power supply to J29. The power supply must be compliant with the TFX12V specification.

Step 4. (*as required*) Connect an RS-232 crossover cable between your test or development host computer and the A34812-ITX. An adapter is required to connect to the UART port.

Step 5. Attach drives to the device. The mapping of drive number to connector is shown in Table 1 in section 4 below.

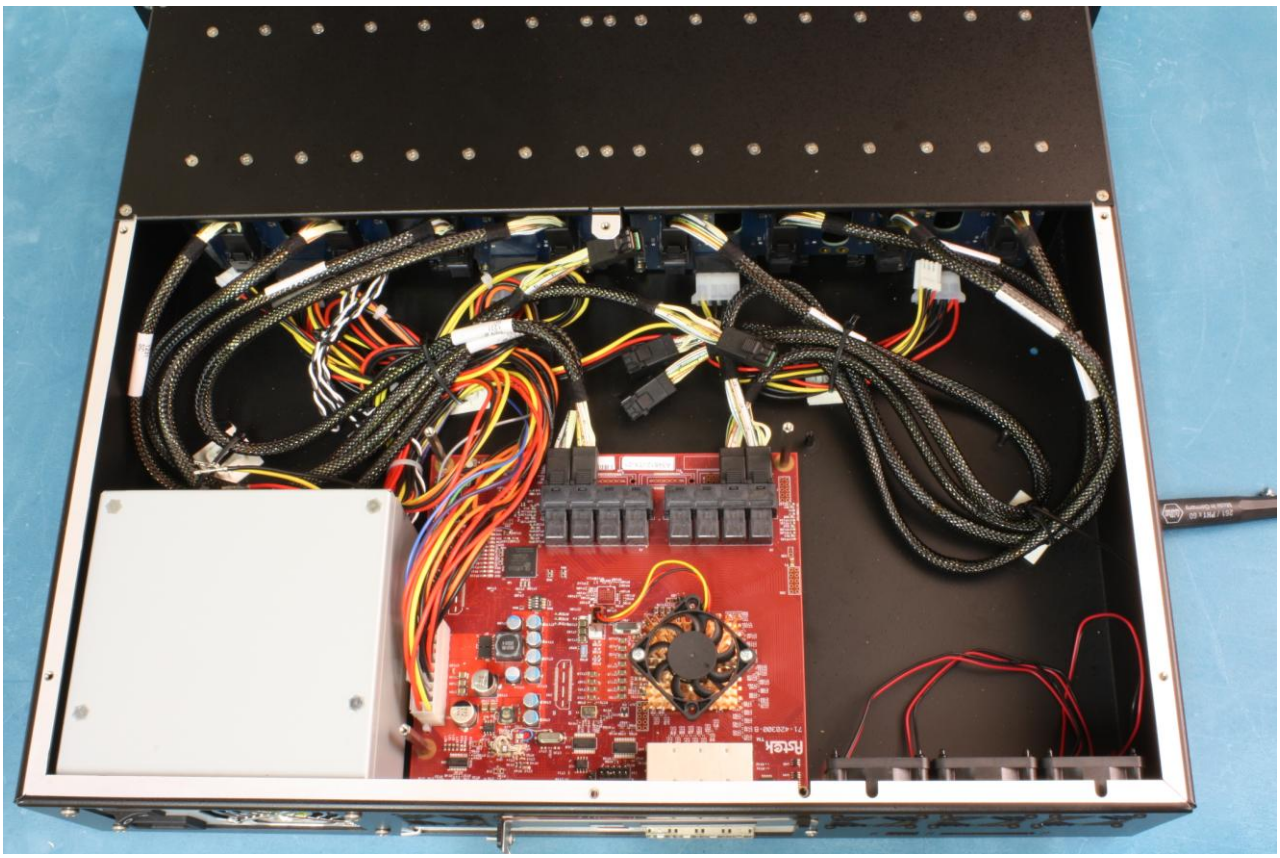
Step 6. Attach connectors from the enclosure front panel indicators (if present) to the Chassis Services header (J27) on the bottom right of the board. Refer to the silkscreen labels on the board and the Front Panel table in Section 4 for pin-out information.

Step 7. Power on the system by pressing the power button on the front panel. NOTE: When using an TFV12V compliant power supply in a system where the expander should be powered whenever AC power is present, place a jumper across pins P13 and P14 on jumper J27.

# 3 Example Use Cases

## JBOD Enclosure

Below illustrates how to connect 16 drives to the A34812-ITX . NOTE: When using a backplane or other signal break-out device for disks attached to the SFF-8643 connectors, SGPIO signals are integrated in the connector and require both a cable with sideband support and a compatible SGPIO target device.  For other SGPIO connection options, contact your Astek sales or engineering representative for support.



# 4 A34812-ITX Single Board Computer Characteristics

## Serial Interfaces

There are two serial ports on the A34812, the smart serial post which is on the external RJ11 connector and the debug serial port on internal J22 header.

### Serial Debug Port

The A34812 expander board provides a Serial Debug UART interface for debug purposes. This Serial Debug UART is entirely implemented in hardware internally and does not require firmware support within the expander, and so can be used even when the firmware does not load successfully. It can be used to program new firmware into an erased or corrupted Flash memory device.

The Serial Debug UART is configured for 8-bit characters, no parity bit, 1 stop bit, and no Xon/Xoff flow control. **Baud rate set to 38400 bps**.

| Pin | Signal Name |
|---|---|
| 1 | UART_TX |
| 2 | open |
| 3 | UART_RX |
| 4 | Ground |

**Table 1: J22 – Serial Debug Port (UART)**

The serial debug port requires an external RS-232 transceiver if you connect the serial debug interface to other RS-232 devices

### Serial Smart Port (UART)

The LSISAS3x48 expander provides an industry-standard UART interface for debug purposes. This UART requires firmware support within the expander, and so cannot be used until the firmware is successfully loaded. The UART is compatible with the standard PC16550D UART and supports the following features.

- The UART supports baud rates up to 115,200 bps. The UART also supports speed sense-logic to automatically determine the connected modem speed.
- The UART supports 8-bit or 7-bit characters. The UART does not support 5-bit or 6-bit characters.
- The UART supports 1 or 2 stop bits. The UART does not support 1.5 stop bits.
- The UART supports even, odd, or no parity bits.
- The UART supports Xon/Xoff flow control or no flow control.
- You can configure the UART to connect internal 16-byte FIFO buffers on the receive input and transmit output.
- The UART provides a synchronous interface to permit access to internal registers and FIFOs.

The A34813 firmware configures the UART for 115,200 bps, 8-bit characters, no parity bit, 1 stop bit, and no Xon/Xoff flow control.

The expander requires an external RS-232 transceiver if you interface the UART to other RS-232 devices.

The standard A34812 firmware, uses this port as a command line interface (CLI) and so it is also known as the Firmware CLI port or the Smart Serial port. The CLI interface has commands to exercise the interfaces within the expander, so it is an effective interface for debugging as well. You can use this interface to update the firmware and manufacturing data easily.

| Pin | Signal Name |
|---|---|
| 1 | UART_RTS |
| 2 | UART_CTS |
| 3 | UART_TX |
| 4 | UART_RX |
| 5 | Ground |
| 6 | Open |

Table 2: J23 – Serial Smart Port (UART) External RJ11

Astek offers a serial cable with a RJ11 connector to DB9 connector. The part number is A40100-CBL-03. This assembly interfaces a standard RS232 cable to a RJ11 connector. The voltage levels on this cable are Standard RS232 levels and this will work on the smart CLI of the A34812.

Useful CLI Commands

| Test | Command |
|---|---|
| Control fan | fan set [duty\|rate\|polarity\|mult\|envppc] [Value(D)] [ID(D)] |
| Read fan setting | fan get [duty\|rate\|polarity\|rpm\|mult\|envppc] [ID(D)] |
| Toggle fan polarity | fan toggle [polarity] [ID(D)] |
| Display SCE topology | scedebug : Prints entire topology information<br>scedebug [exp] : All expanders only<br>scedebug [dev] : All attached devices only<br>scedebug [exp] [SASAddrHigh(H)] [SASAddrLow(H)] :<br>Given expander information only<br>scedebug [expdev] [SASAddrHigh(H)] [SASAddrLow(H)] :<br>Given expander or attached device information |
| Mirror enable | mirror enable [SourcePhy(D)] [TxDestPhy(D)] [RxDestPhy(D)] |
| Mirror disable | mirror disable [SourcePhy(D)] |
| Mirror status | mirror status |
| Route table read | rtr [Display(d\|z\|dz)](opt)<br>Default display enabled entries with a nonzero SAS address<br>d include disabled entries<br>z include entries with a zero SAS address<br>dz display all entries |
| Read zone permissions | rperm [SourceZoneGroup(H)] |
| Show the current logs | showlogs [DisplayMode(hex\|detail\|default)](opt) |
| Clear the logs | clearlogs |
| Log a string | log [String] |

| | |
|---|---|
| File download | fdl [BufferID(H)] [Offset(H)] [Erase(Y\|N)](opt) |
| File upload | ful [BufferID(H)] [Offset(H)] [Size(D)](opt) |
| Display cable management info | cableinfo [PhyIndex(D)] |
| Show wide port power management info | wppminfo |
| Display info for all phys | phyinfo [help\|power\|cable](opt) [up\|PhyNum(D)](opt)<br>no arguments displays default output<br>'help' displays detailed help information<br>'power' subcommand displays power mgmt info<br>'up' filters to display connected phys only<br>'cable' subcommand displays cable mgmt info<br><PhyNum> is a valid phy index and filters the output to display info about that phy |
| Display or reset all phy counters | counters [config\|event\|reset](opt)<br>no arguments displays phy error counters and generic broadcast counters<br>'config' subcommand displays phy event configuration<br>'event' subcommand displays phy event counters<br>'reset' subcommand resets all phy counters |
| Display expander SAS address | sasaddr |
| Show network info | ipconfig |
| Close TCP/IP session | exit |
| Show manufacturing rev | showmfg |
| Show firmware rev | rev |
| CLI Help | help [Command](opt)<br>[X] means an argument described as x<br>[X](opt) means an optional argument<br>[X(D)] means a decimal value<br>[X(H)] means a hexadecimal value<br>[X(s)] means a decimal value in seconds<br>[X(ms)] means a decimal value in milliseconds<br>[X(val1-val2)] means a value between val1 and val2<br>[X(opt1\|opt2\|opt3)] means opt1,opt2, or opt3<br>[X1] [X2] ... means a variable number of arguments |

# Power and Cooling

- Power for the A34812-ITX is supplied by a single 20-pin TFX12V compatible power connector.
- The A34812-ITX provides eight connectors, seven usable for enclosure cooling.

## Input Power Connector

The Power connector J29 is compatible with the TFX12V standard, and can support either a 20 pin or 20+4 pin modular cable. Power may be either continuous, or controlled remotely using the standard TFX12V PS_ON# signal of the J29 connector. If remote power control is used, the chassis must connect a switch to pins 16 and 14 of J27 (see section Other Headers). NOTE: The 3.3VDC, -12VDC and -5VDC inputs are unused with the A34812-ITX board and may be omitted for cost savings.

| Pin | Signal Name | | Pin | Signal Name |
|---|---|---|---|---|
| 11 | | | 1 | 3.3V (unused) |
| 12 | -12V (unused) | | 2 | 3.3V (unused) |
| 13 | GND | | 3 | GND |
| 14 | PS_ON# | | 4 | V5.0 |
| | GND | | 5 | GND |
| 16 | GND | | 6 | V5.0 |
| 17 | GND | | 7 | GND |
| 18 | -5V (unused) | | 8 | PWR_OK |
| 19 | V5.0 | | 9 | V5.0_STBY |
| 20 | V5.0 | | 10 | V12 |

**Table 3: J29 - Power Header Pinout**

## Cooling Fan Connectors

There are 8 total (J4, J5, J6, J7, J9, J26, J36, J37) on the A34812-ITX board, 7 of these are user-accessible chassis cooling fan outputs, with one header attached to the fan-sink for the SAS3x48 device as delivered (J6)[1]. These connectors support two-pin (fan w/o sensor), three-pin (fan w/ rotation sensor), or four pin devices (variable speed fan[2] w/ rotation sensor). By default all fan outputs will be configured for full speed operation at start. For information about software control over these fans contact your Astek or OEM sales representative for information about the SCSI Enclosure Services capabilities of the LSISAS3x48 SDK. NOTE: J4, J5 and J7 are driven by an on-board ADT7476 thermal sense and PWM controller device. This device can be configured for "automatic" thermal regulation of the PWM fans. Astek recommends that these headers be used in preference to the additional headers during chassis design.

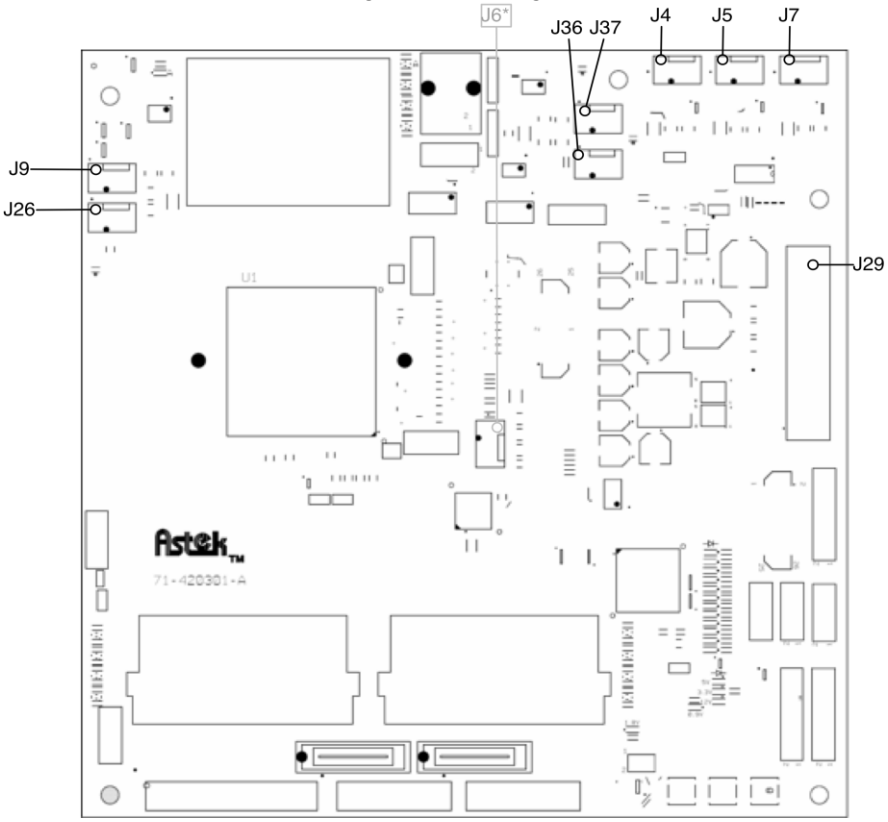



**Illustration 2: A34812-ITX Board Layout and Connector Locations**

| Pin | Signal Name |
|---|---|
| 1 | GND |
| 2 | 12V |
| 3 | TACH |
| 4 | PWM |

**Table 4: J4,J5,J6,J7,J9,J26,J36,J37 - 4-pin Fan Header Pinout**

1 Do not disconnect **this fan-sink unless you can ensure that sufficient air-flow is maintained across the heat-sink for the LSISAS3x48. Warranty is** void unless modification is approved in writing by Astek.

2 Fan devices must comply with the "4-Wire Pulse Width Modulation (PWM) Controlled Fans" available from http://www.formfactors.org/.

## LED s and Indicators

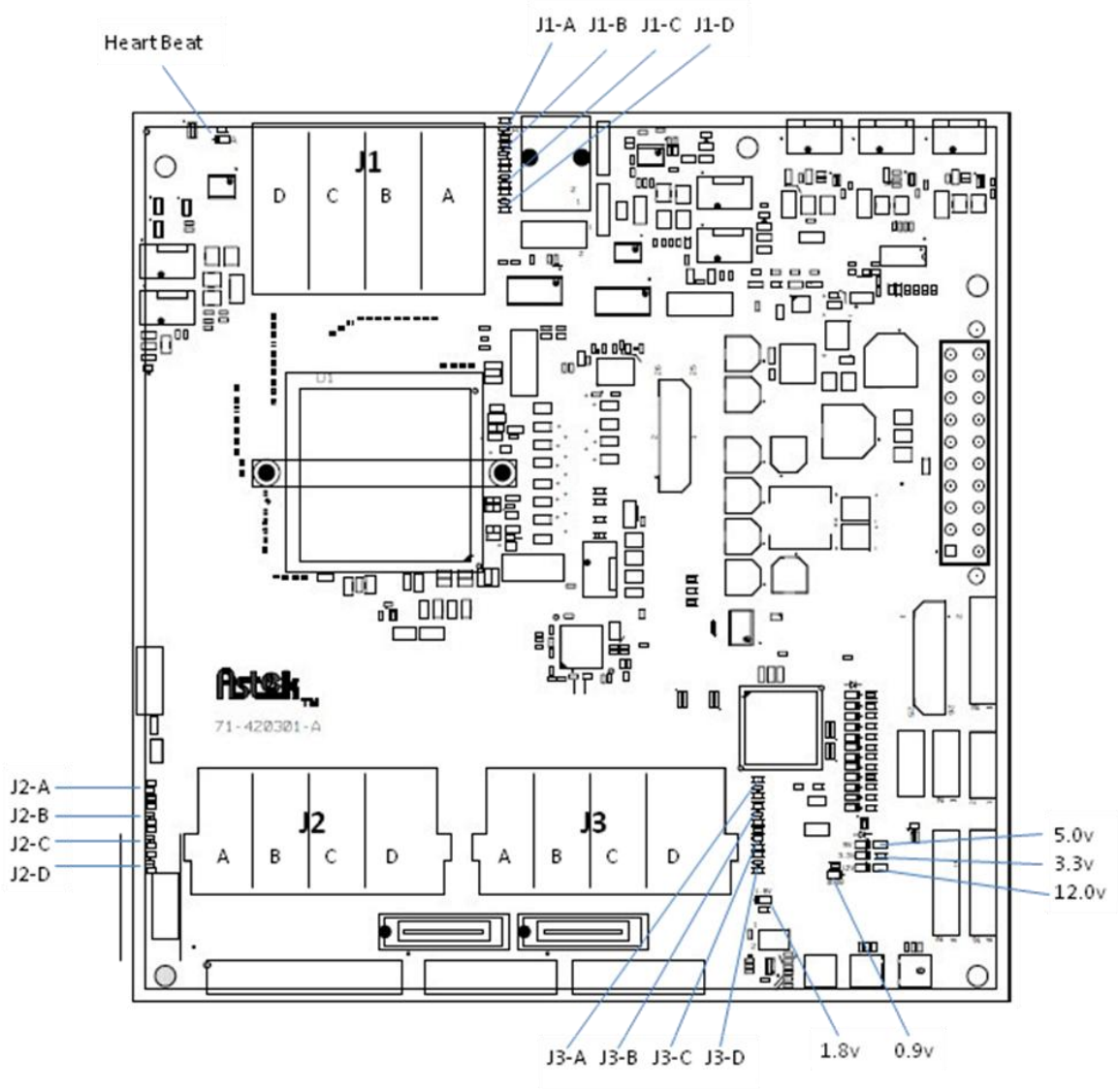



**Illustration 3: LED Indicators**

## SAS Bus Interfaces

All SAS lanes are routed to internal or external Mini-SAS HD connectors for connectivity to either disks, hosts, cascaded expanders, or any combination of these connection types (see Illustration 6: SAS Internal and External Connectors below).

### External Connector

There is a single quad SFF-8644 Mini-SAS HD external connector (J1) housing on the bulkhead edge of the A34812-ITX board. The side-band signals on this connector are configured to support the use of active/powered cables complying with the SAS r3.0 specification. Support for cables may require special SAS3x48 firmware, contact your Astek engineering representative for assistance.

## Internal Connectors

There are two quad SFF-8643 internal Mini-SAS HD connector housings (J2 and J3) on the internal edge of the A34812-ITX board. The side-band signals on these connectors are configured to support SGPIO output for compatible break-out/backplanes. Support requires a cable with side-band signals and a compatible SGPIO target device – for a list of compatible SGPIO devices or assistance with backplane design and qualification, see your Astek engineering representative. NOTE: PHY lanes 40 through 47 are not present on boards which use the less expensive LSISAS3x40 device, however the same modular connector is used for both boards (see pinout for which gangs are no-connect with this variant). The internal SAS receptacles are wired according to the ANSI T10 SAS3.0 specification for internal SFF-8643 connectors supporting SGPIO side-band signaling (see SFF-8485 for electrical and protocol specification).

## SAS Receptacle Lane Mapping

The SAS receptacles are wired to the following numbered SAS PHY lanes as follows:

| Label | Conn. Lane ↔ Phys | | | | Connector Type | Recommended Connection | Sideband Pin Function | Comments |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | | | | |
| J1/A | 13 | 12 | 14 | 15 | SFF-8644 | Host | Active/Powered Cable | |
| J1/B | 17 | 16 | 18 | 19 | SFF-8644 | Host | Active/Powered Cable | |
| J1/C | 21 | 20 | 22 | 23 | SFF-8644 | Host | Active/Powered Cable | |
| J1/D | 25 | 24 | 26 | 27 | SFF-8644 | Host | Active/Powered Cable | |
| J2/A | 33 | 32 | 34 | 35 | SFF-8643 | Host | SGPIO (4 elements) | |
| J2/B | 37 | 36 | 38 | 39 | SFF-8643 | Host | SGPIO (4 elements) | |
| J2/C* | 41 | 40 | 42 | 43 | SFF-8643 | Devices | SGPIO (4 elements) | *No connect for A34012 |
| J2/D* | 45 | 44 | 46 | 47 | SFF-8643 | Devices | SGPIO (4 elements) | *No connect for A34012 |
| J3/A | 29 | 28 | 30 | 31 | SFF-8643 | Devices | SGPIO (4 elements) | |
| J3/B | 1 | 0 | 2 | 3 | SFF-8643 | Devices | SGPIO (4 elements) | |
| J3/C | 5 | 4 | 6 | 7 | SFF-8643 | Devices | SGPIO (4 elements) | |
| J3/D | 9 | 8 | 10 | 11 | SFF-8643 | Devices | SGPIO (4 elements) | |

**Table 5: SAS Connector Pinout and Suggested Connectivity**

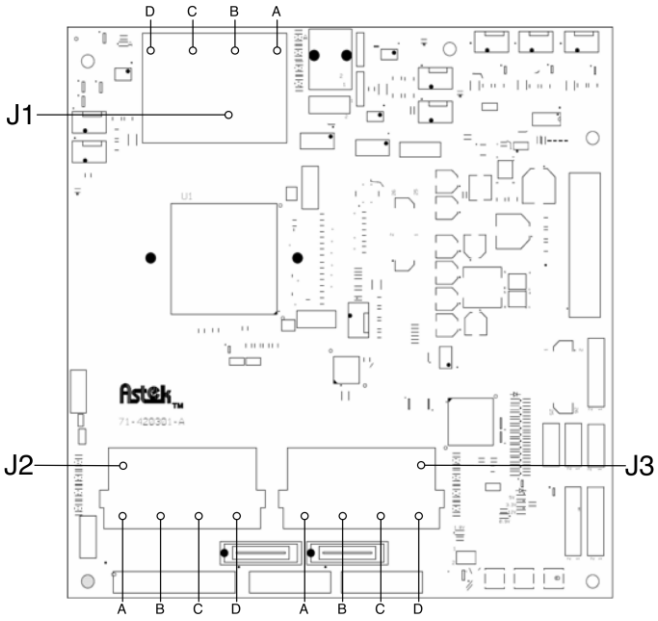



**Illustration 4: SAS Internal and External Connectors**

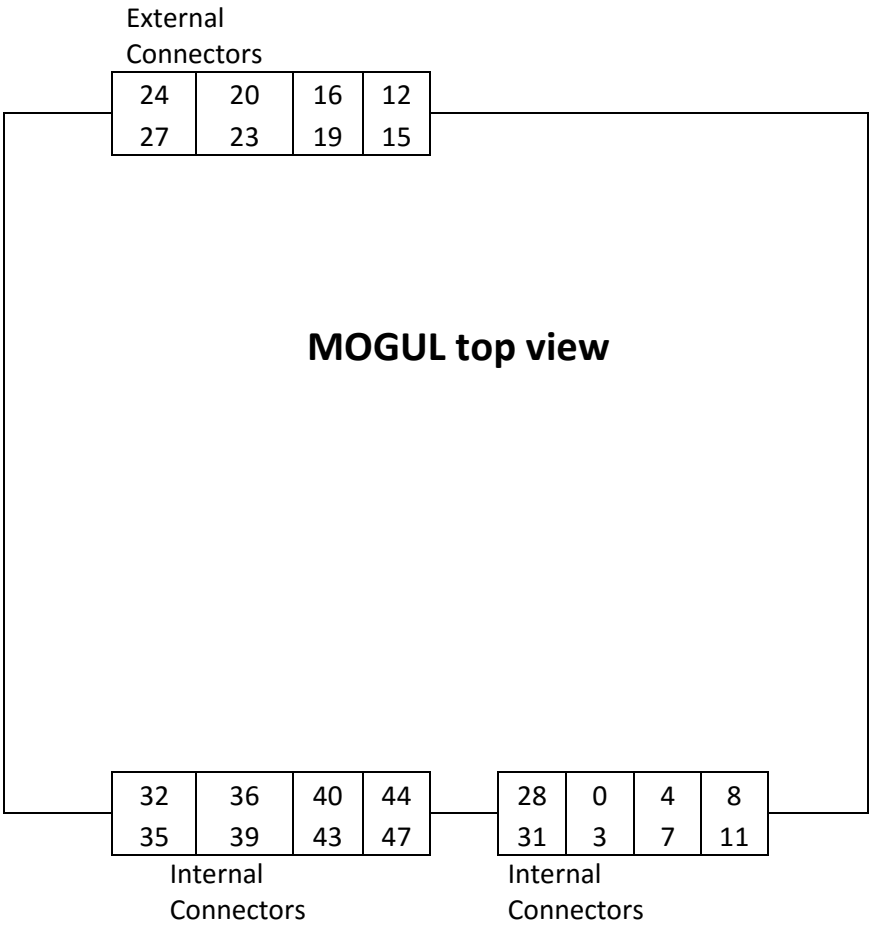
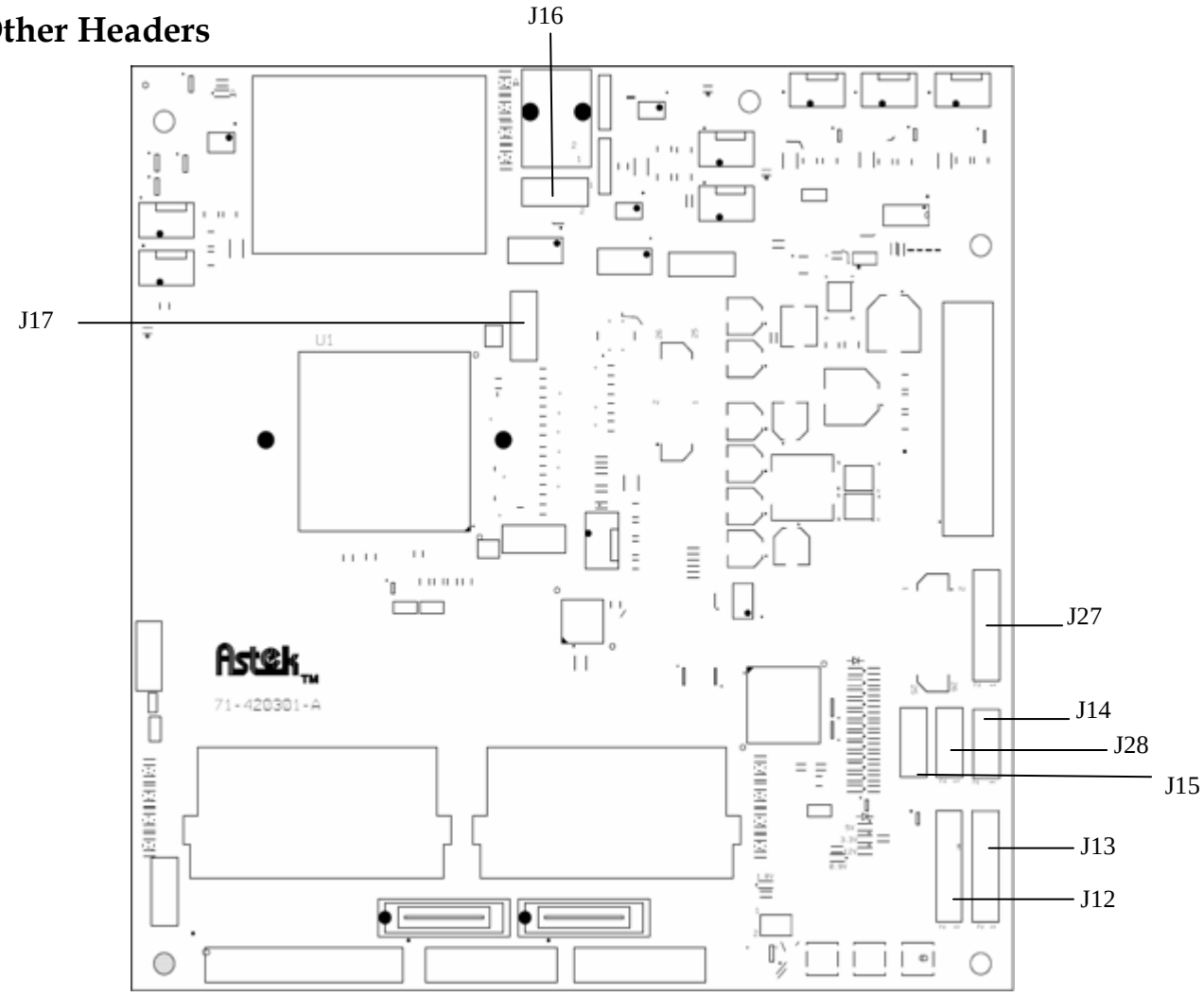



**Illustration 5: SAS Internal and External Phys Connections**

## Other Headers




J12

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 2 | GND | FPGA_GPIO[1] | 1 |
| 4 | GND | FPGA_GPIO[2] | 3 |
| 6 | V3.3 | FPGA_GPIO[3] | 5 |
| 8 | GND | FPGA_GPIO[4] | 7 |
| 10 | GND | FPGA_GPIO[5] | 9 |
| 12 | V3.3 | FPGA_GPIO[6] | 11 |
| 14 | GND | FPGA_GPIO[7] | 13 |
| 16 | GND | Powerfail | 15 |

J13

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 2 | GND | FPGA_GPIO[8] | 1 |
| 4 | GND | FPGA_GPIO[9] | 3 |
| 6 | V3.3 | FPGA_GPIO[10] | 5 |
| 8 | GND | FPGA_GPIO[11] | 7 |
| 10 | GND | FPGA_GPIO[12] | 9 |
| 12 | V3.3 | FPGA_GPIO[13] | 11 |
| 14 | GND | FPGA_GPIO[14] | 13 |
| 16 | GND | FPGA_GPIO[15] | 15 |

J14

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 2 | FGPA_SGPIO_LD_OUT[8] | FGPA_SGPIO_DATA_OUT[8] | 1 |
| 4 | FGPA_SGPIO_DATA_IN[8] | FGPA_SGPIO_LD_IN[8] | 3 |
| 6 | FGPA_SGPIO_CLK_OUT[8] | FGPA_SGPIO_CLK_IN[8] | 5 |
| 8 | GND | GND | 7 |
| 10 | V3.3 | V3.3 | 9 |

J15

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 2 | FGPA_SGPIO_LD_OUT[9] | FGPA_SGPIO_DATA_OUT[9] | 1 |
| 4 | FGPA_SGPIO_DATA_IN[9] | FGPA_SGPIO_LD_IN[9] | 3 |
| 6 | FGPA_SGPIO_CLK_OUT[9] | FGPA_SGPIO_CLK_IN[9] | 5 |
| 8 | GND | GND | 7 |
| 10 | V3.3 | V3.3 | 9 |

J16

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 2 | IIC_SCL[5] | IIC_SCL[1] | 1 |
| 4 | IIC_SDA[5] | IIC_SDA[1] | 3 |
| 6 | GND | GND | 5 |
| 8 | IIC_SDA[4] | IIC_SDA[0] | 7 |
| 10 | IIC_SCL[4] | IIC_SCL[0] | 9 |

J17

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 2 | IIC_SCL[7] | IIC_SCL[3] | 1 |
| 4 | IIC_SDA[7] | IIC_SDA[3] | 3 |
| 6 | GND | GND | 5 |
| 8 | IIC_SDA[6] | IIC_SDA[2] | 7 |
| 10 | IIC_SDA[6] | IIC_SCL[2] | 9 |

J27

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 2 | LAN2_LED_A | LAN1_LED_A | 1 |
| 4 | FPGA_SPARE[0] | FPGA_SPARE[1] | 3 |
| 6 | P_LED_ANODE | HDD_LED_ANODE | 5 |
| 8 | NC | FPGA_SPARE[2] | 7 |
| 10 | P_LED_CATHODE (GND) | NC | 9 |
| 12 | PS_ON# | GND | 11 |
| 14 | GND | GND | 13 |
| 16 | IO SWITCH | SW_POR_RST | 15 |

J28

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 2 | SIO_LD_OUT_LS | SIO_D_OUT_LS | 1 |
| 4 | SIO_D_IN_LS | SIO_LD_IN_LS | 3 |
| 6 | SIO_CLK_OUT_LS | SIO_CLK_IN_LS | 5 |
| 8 | GND | GND | 7 |
| 10 | V3.3 | V3.3 | 9 |

# 5 Specifications

## Electrical Specifications

### Power

- Operating Voltage Limits:
  - +12VDC +/- 10%
  - +5VDC +/- 10%
  - +5VSB +/- 10%
- Typical Power Consumption:
  - (16-lanes SAS @12Gbps, 24-lanes SAS @ 6Gbps)
  - 30W Nominal
- Maximum Power Consumption:
  - (48-lanes SAS @ 12Gbps)
  - 36W Estimated
- Power Connector:
  - 20-pin TFX12V header, compatible with 24-pin cables

## Environmental Specifications

### Operating Conditions

- Temperature:
  - 0 °C to +55 °C
- Humidity:
  - 5 to 90% non-condensing
- Airflow:
  - No additional airflow required when used with supplied active fan-sink device

### Storage Conditions

- Temperature:
  - -45 °C to +55 °C
- Humidity:
  - 5 to 90% non-condensing

| | |
|---|---|
| CAUTION | Do not operate the A34812-ITX continuously without sufficient cooling. The default configuration does NOT support auto-shutdown due to exceeding thermal limits, and as such, damage many occur to your board if operated continuously without airflow. |

# Mechanical Specifications

This A34812-ITX conforms to the Mini-ITX specification regarding board size and mounting hole locations. The mounting holes accept M3 hardware.

## Dimensions

| | |
|---|---|
| Height: | 170.0 mm (6.69 inches) |
| Length: | 170.0 mm (6.69 inches) |

## Mounting Holes Drawing

The board can be mounted in a chassis using the 4 mounting holes shown below example board.

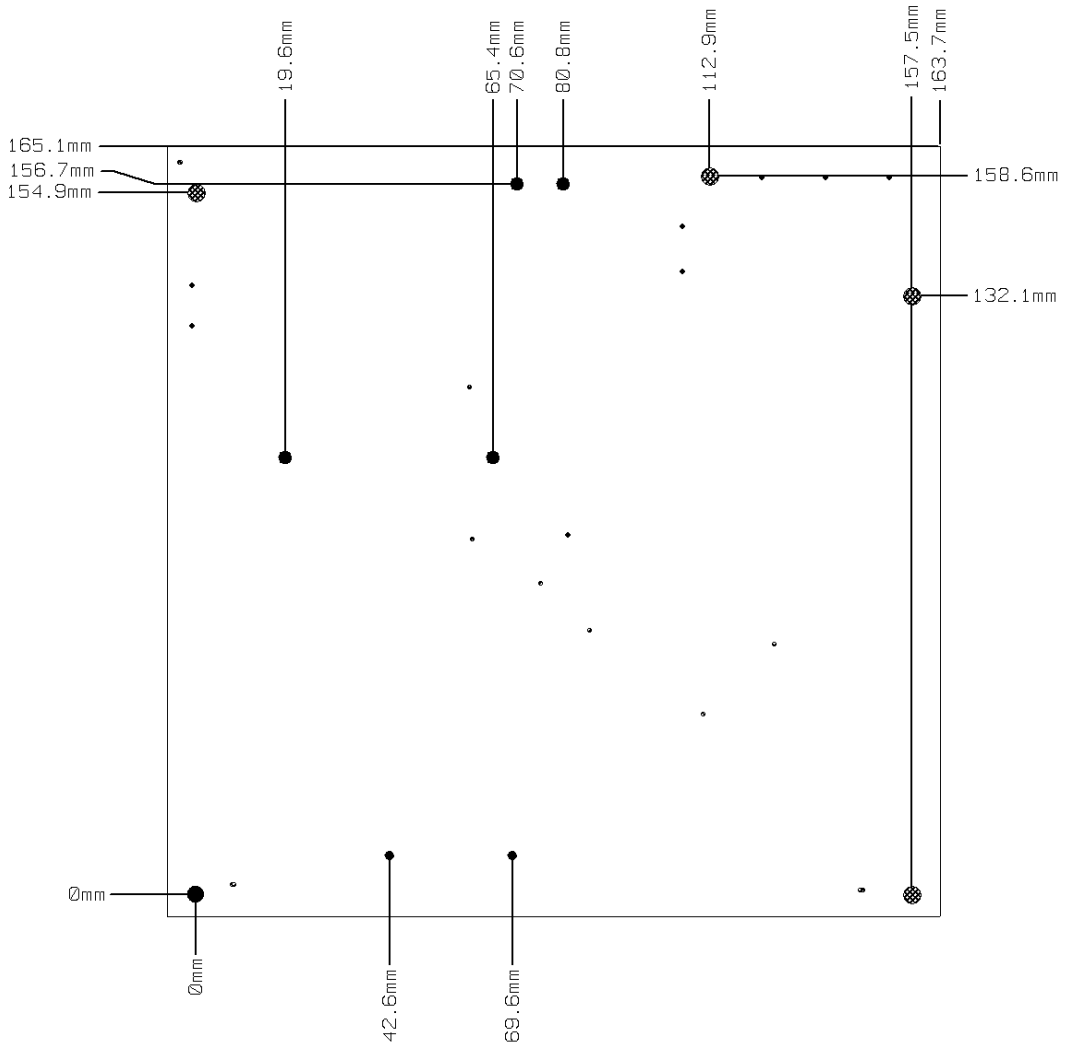



**Illustration 6: Mounting Hole Locations**

# 6 Troubleshooting

## Diagnostics

The following diagnostic tests may be helpful in the event that the A34812-ITX board is not operating as expected.

- Verify that +5VSB standby power,+5VDC and +12VDC supply power are available on the 20-pin power connector.
- Look for the heartbeat LED indicator (corner marked D14), this should be pulsing at approximately 1Hz rate.
- For SAS connectivity, there are LED indicators on the board. External lane indicators are located between J1 and J16. Internal lane indicators are located to the right side of J3 when looking at internal connectors.
    - Each connector (x4 link) has a single indicator for “FAULT” state (ie: no SAS/SATA link), any PHY in the x4 link that is disconnected will cause the LED to be lit (RED)
    - Each connector (x4 link) has a single activity indicator, any traffic will cause the LED to be lit or pulse (green)

## Support

For additional support, contact your Product Manager or email support@astekcorp.com.

Astek can be contacted at (719) 260-1625 or toll-free at (800) 850-9055.