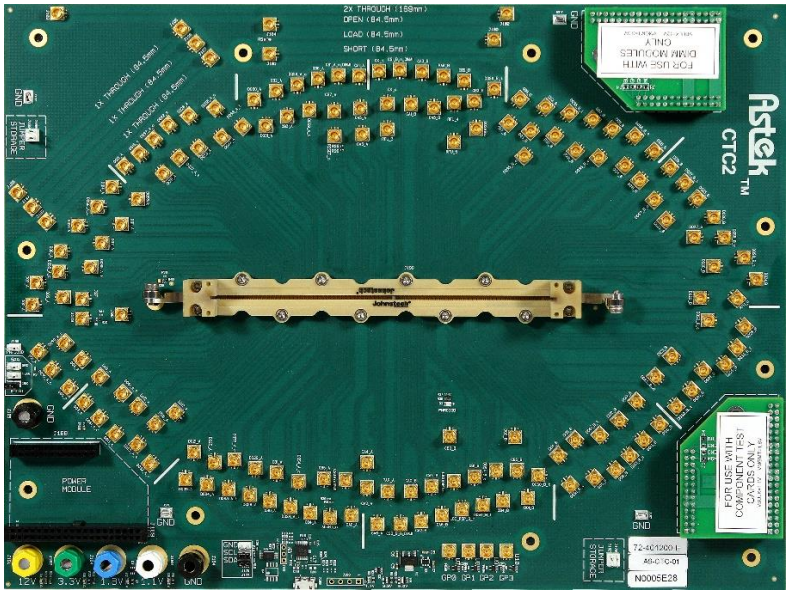
A9-CTC2

User Manual

Version: **June 24, 2019**

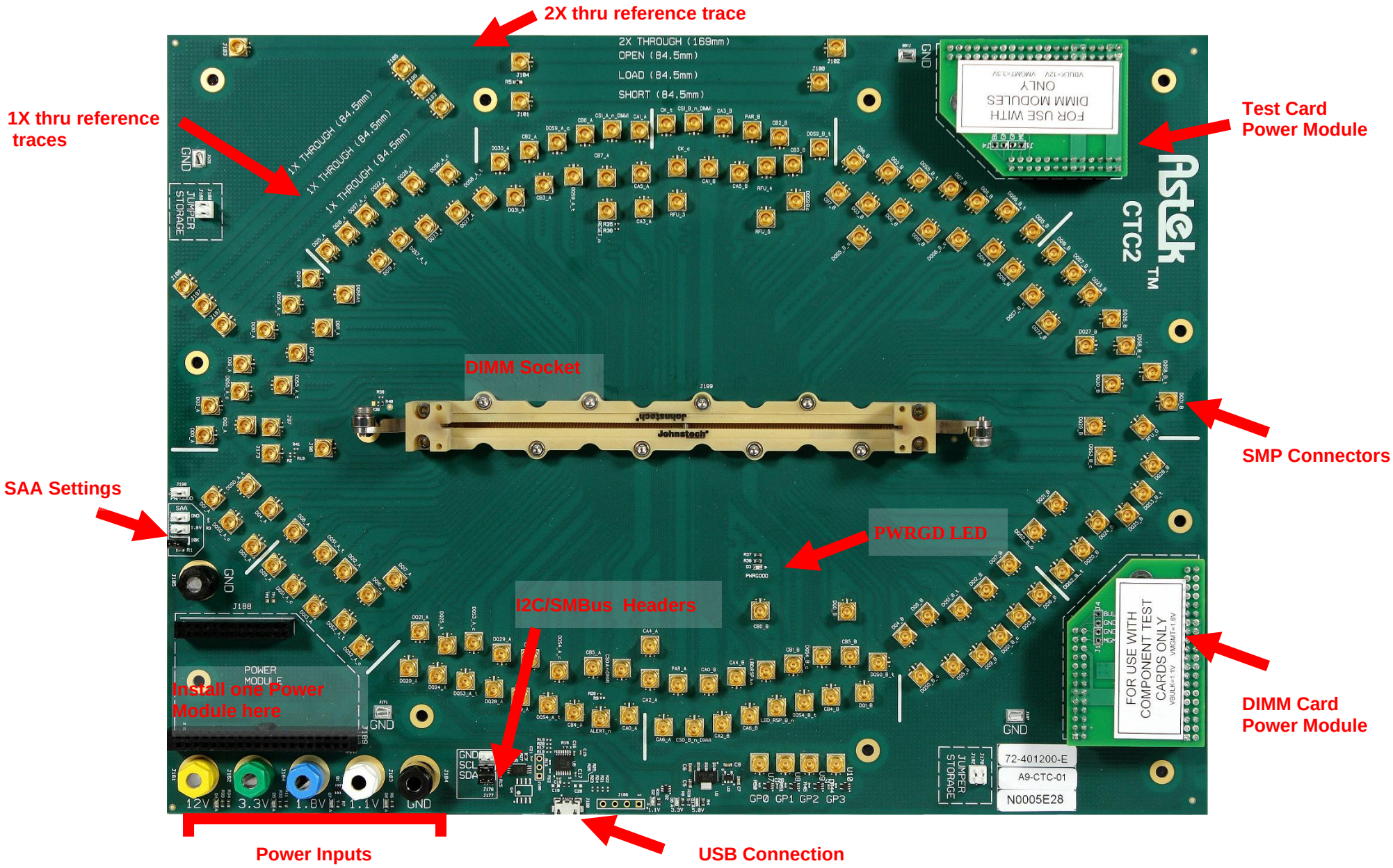


To receive product literature, visit us at http://www.astekcorp.com.

1 Introduction / Overview

This document outlines the features and use of Astek's Channel Test Card 2 (CTC2). The CTC2 provides signal access for testing DDR5 DIMMs and component test cards using oscilloscopes, BERTs, and signal generating test equipment. The CTC2 provides access via SMP connectors to all signals on a DIMM connector. The CTC2 can be configured with no DIMM socket, a high-performance socket, or a standard socket.

Each signal is 50-ohms and all signals are matched to within +/- 1mil tolerance. Every signal is brought out to an SMP connector or a header.



2 Optional Equipment

Astek DIMM Parametric Card
The DIMM Parametric Card can be used for advanced characterization of the CTC2 board and is useful for changing the reference plane to other locations in the test system.

Astek Reset Automation Board
Automate reset sequencing of board

Astek Controller Board
Astek provides a controller board used to configure a DRAM device installed on a test card inserted into the CTC2.

Micro USB cable
A micro USB cable can be used to connect the CTC2 to a host PC. The USB interface provides a method of configuring a DIMM or test card during characterization testing.

I2C host
An I2c host, such as TotalPhase Aardvark, can be used to configure a DIMM or test card during characterization testing.

SMP cabling
SMP cables are needed to connect the CTC2 to test equipment or other test hardware. Depending on the equipment and connectivity needs, either SMP to SMP cables or SMP to SMA cables are needed.

Power Supply
A dual-port power supply is required to power the device under test. For DIMM cards, 3.3V and 12V are required. For device test cards, 1.1V and 1.8V are required.

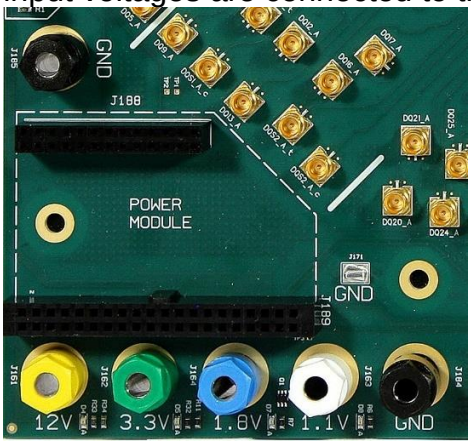
Test equipment
Depending on the characterization needs, various test equipment such as oscilloscopes, bit-error rate testers (BERTs), and pattern generators are used to drive stimulus and monitor the output of devices under test.

Contact your Astek representative for information and quotations for the optional equipment listed above.

3 Powering the CTC2

The CTC2 is designed to support testing of DIMM cards requiring 3.3V and 12V and component test cards requiring 1.1V and 1.8V. Power for the device under test is controlled by inserting the correct power module onto the CTC2 and applying the appropriate power to the banana jacks.

The power module is installed in the lower right corner of the PCB and determines which input voltages are connected to the device under test.



Voltage Pin	Voltage Level	Adapter Board	Banana Jack	Color
VIN BULK	12V	DIMM Adapter Board	12V @ J161	Yellow
VIN MGMT	3.3V		3.3V @ J162	Green
VIN BULK	1.1V	Test Card Adapter Board	1.1V @ J163	White
VIN MGMT	1.8V		1.8V @ J164	Blue

DIMM Card testing

When testing DIMM cards, install the power module labeled “FOR USE WITH DIMM CARDS ONLY”. When the DIMM power adapter is installed, 3.3V is applied to VIN_MGMT and 12V is applied to VIN_BULK.

If the USB cable is connected to a PC, the LEDs near 3.3V and 12V will illuminate.

Component Test Card testing

When testing component test cards, install the power module labeled “FOR USE WITH TEST CARDS ONLY”. When the Test Card power adapter is installed, 1.8V is applied to VIN_MGMT and 1.1V is applied to VIN_BULK.

If the USB cable is connected to a PC, the LEDs near 1.1V and 1.8V will illuminate.

4 Signals Probed

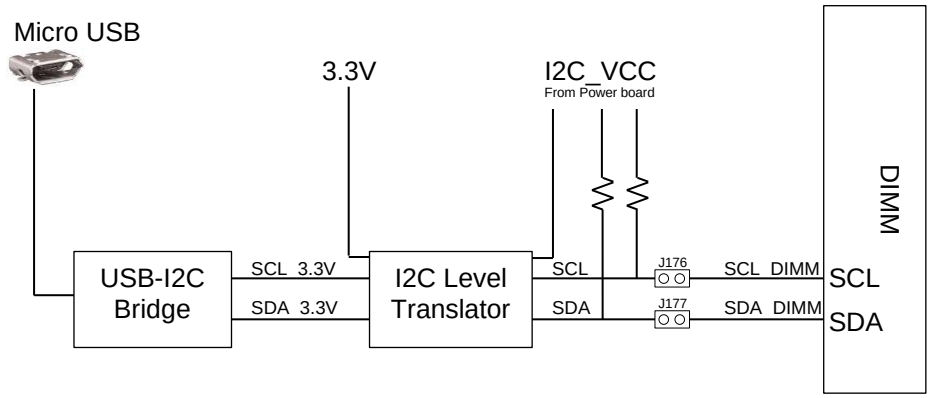
The following signals are brought out to SMP Connectors on the CTC2

Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin
ALERT_n	62	CB0_A	51	CK_c	218	DQ0_A	7	DQ10_A	163	DQ21_A	38	DQS0_A_c	12	DQS5_A_c/TDQS5_A_c	156
CA0_A	66	CB0_B	89	CK_t	217	DQ0_B	100	DQ10_B	256	DQ21_B	131	DQS0_A_t	11	DQS5_A_t/TDQS5_A_t/DBI0_A_n	157
CA0_B	78	CB1_A	53	CS0_A_n	64	DQ1_A	9	DQ11_A	165	DQ22_A	181	DQS0_B_c	105	DQS5_B_c/TDQS5_B_c	249
CA1_A	211	CB1_B	91	CS0_B_n	76	DQ1_B	102	DQ11_B	258	DQ22_B	274	DQS0_B_t	104	DQS5_B_t/TDQS5_B_t/DBI0_B_n	250
CA1_B	223	CB2_A	196	CS1_A_n	209	DQ2_A	152	DQ12_A	25	DQ23_A	183	DQS1_A_c	23	DQS6_A_c/TDQS6_A_c	167
CA2_A	68	CB2_B	234	CS1_B_n	221	DQ2_B	245	DQ12_B	118	DQ23_B	276	DQS1_A_t	22	DQS6_A_t/TDQS6_A_t/DB11_A_n	168
CA2_B	80	CB3_A	198	PAR_A	74	DQ3_A	154	DQ13_A	27	DQ24_A	40	DQS1_B_c	116	DQS6_B_c/TDQS6_B_c	260
CA3_A	213	CB3_B	236	PAR_B	229	DQ3_B	247	DQ13_B	120	DQ24_B	133	DQS1_B_t	115	DQS6_B_t/TDQS6_B_t/DB11_B_n	261
CA3_B	225	CB4_A	58	RESET_n	207	DQ4_A	14	DQ14_A	170	DQ25_A	42	DQS2_A_c	34	DQS7_A_c/TDQS7_A_c	178
CA4_A	70	CB4_B	96	LBD/RSP_A_n	86	DQ4_B	107	DQ14_B	263	DQ25_B	135	DQS2_A_t	33	DQS7_A_t/TDQS7_A_t/DB12_A_n	179
CA4_B	82	CB5_A	60	LBS/RSP_B_n	87	DQ5_A	16	DQ15_A	172	DQ26_A	185	DQS2_B_c	127	DQS7_B_c/TDQS7_B_c	271
CA5_A	215	CB5_B	98	RFU_0	144	DQ5_B	109	DQ15_B	265	DQ26_B	278	DQS2_B_t	126	DQS7_B_t/TDQS7_B_t/DB12_B_n	272
CA5_B	227	CB6_A	203	RFU_1	149	DQ6_A	159	DQ16_A	29	DQ27_A	187	DQS3_A_c	45	DQS8_A_c/TDQS8_A_c	189
CA6_A	72	CB6_B	241	RFU_2	150	DQ6_B	252	DQ16_B	122	DQ27_B	280	DQS3_A_t	44	DQS8_A_t/TDQS8_A_t/DB13_A_n	190
CA6_B	84	CB7_A	205	RFU_3	220	DQ7_A	161	DQ17_A	31	DQ28_A	47	DQS3_B_c	138	DQS8_B_c/TDQS8_B_c	282
		CB7_B	243	RFU_4	231	DQ7_B	254	DQ17_B	124	DQ28_B	140	DQS3_B_t	137	DQS8_B_t/TDQS8_B_t/DB13_B_n	283
				RFU_5	232	DQ8_A	18	DQ18_A	174	DQ29_A	49	DQS4_A_c	56	DQS9_A_c/TDQS9_A_c	200
				FAIL_n	147	DQ8_B	111	DQ18_B	267	DQ29_B	142	DQS4_A_t	55	DQS9_A_t/TDQS9_A_t/DB14_A_n	201
						DQ9_A	20	DQ19_A	176	DQ30_A	192	DQS4_B_c	94	DQS9_B_c/TDQS9_B_c	238
						DQ9_B	113	DQ19_B	269	DQ30_B	285	DQS4_B_t	93	DQS9_B_t/TDQS9_B_t/DB14_B_n	239
								DQ20_A	36	DQ31_A	194				
								DQ20_B	129	DQ31_B	287				

5 I2C

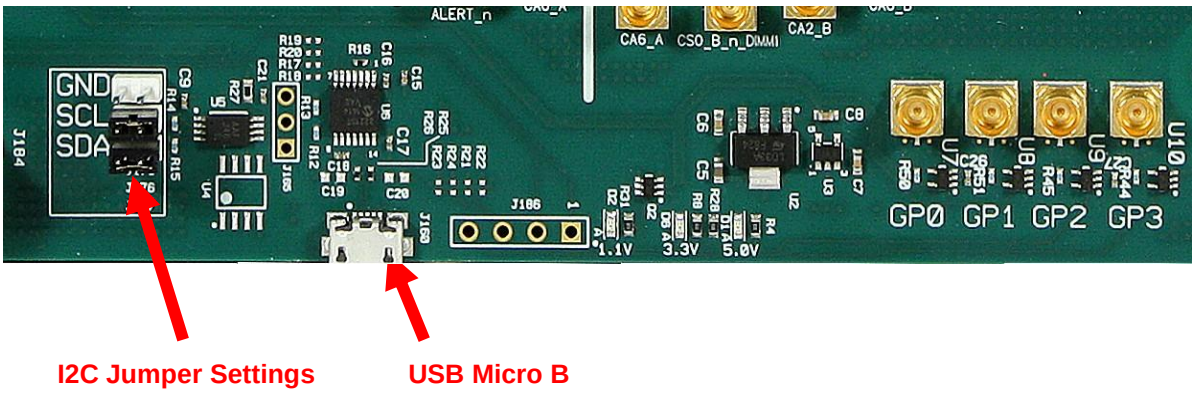
I2C Circuitry

Block Diagram of the I2C circuitry on the CTC2 is shown below.



The CTC2 uses a Micro B USB connector to access the I2C/SMBus bus on the DDR5 socket. (SDA – Pin 5, SCL – Pin 4)

The location of the USB Micro B connector and I2C support circuitry is shown below.

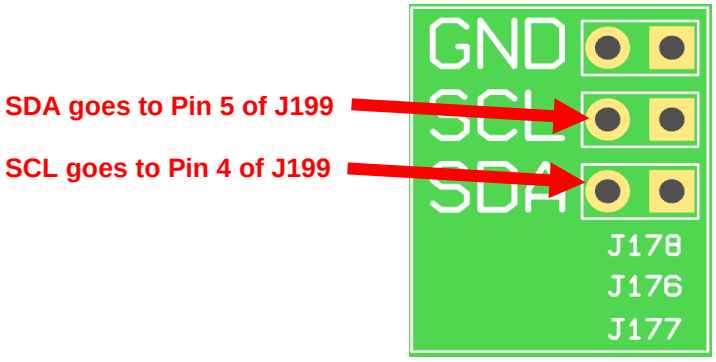


The I2C_VCC pull-up voltage is automatically set based on which Power Adapter board is installed on the CTC2.

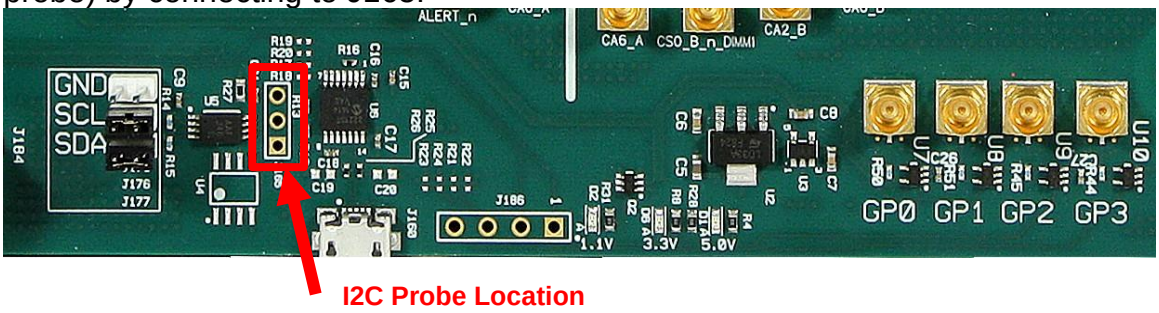
Test Card Adapter Board	1.8V
DIMM Adapter Board	1.1V

By default, the jumpers J176 and J177 are installed. When J176 and J177 are installed, the I2C bus is driven via the USB-to-I2C bridge.

To access the I2C pins directly on the DDR5 DIMM, remove jumpers on J176 and J177 and attach directly to the I2C pins as shown below. When the jumpers are removed, the on-board pullups are also removed from the circuit (see the block diagram above).



The I2C bus may be probed with an I2C protocol analyzer (such as the Saleae Logic 8 probe) by connecting to J165.



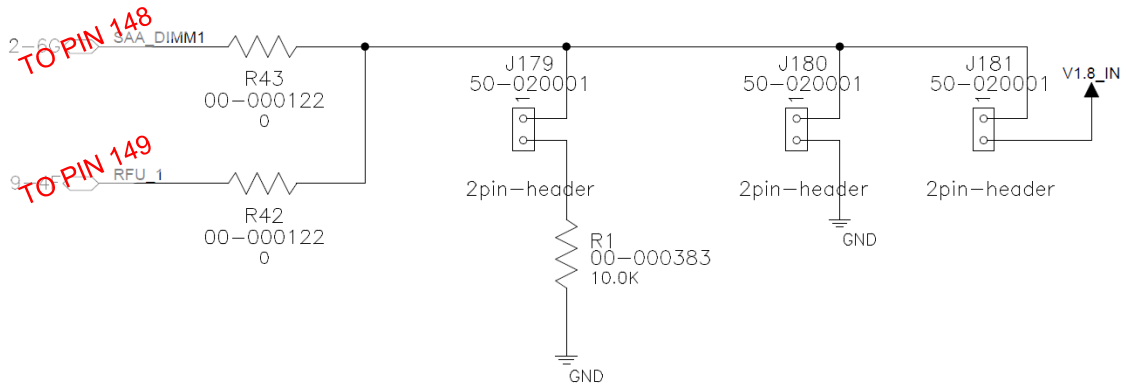
The pinout of J165 is:

Pin	Signal
1	SDA
2	SCL
3	GND

SAA Circuitry

The SAA pin circuitry on the CTC2 provides the option to change the connection point to the DIMM connector (pin 148 or pin 149) and to change the HOSTID provided to the DIMM.

The SAA circuitry is shown below.



The following table determines the HOSTID indicated to a DIMM plugged into the system.

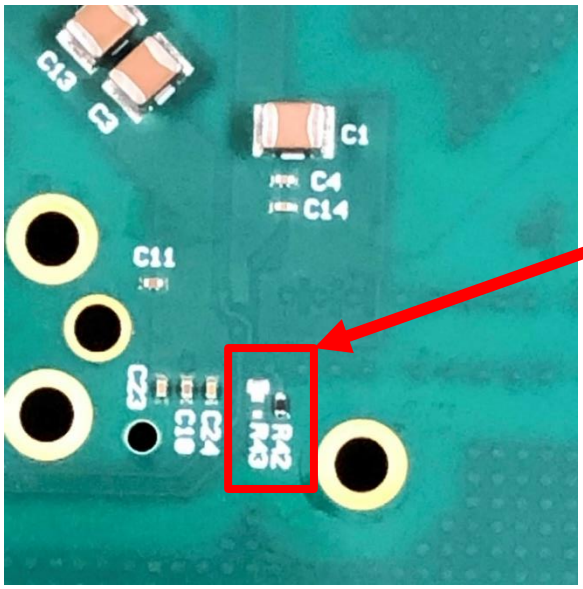
Resistor Value		Meaning
10,000 Ω	(R1)	HOST ID = 000 (default)
15,400 Ω	(R1)	HOST ID = 001
23,200 Ω	(R1)	HOST ID = 010
35,700 Ω	(R1)	HOST ID = 011
54,900 Ω	(R1)	HOST ID = 100
84,500 Ω	(R1)	HOST ID = 101
127,000 Ω	(R1)	HOST ID = 110
196,000 Ω	(R1)	HOST ID = 111
VSS	(J180)	HOST ID = 000
VDDSPD	(J181)	HOST ID = 000

To use a resistor to select the HOST ID, remove J180 and J181 and install J179 (default configuration) and change R1 to the desired value. R1 is located near the SAA jumpers.

To set the HOST ID using VSS, remove J179 and J181 and install J180.

To set the HOST ID using VDDSPD, remove J179 and J180 and install J181.

SAA PIN LOCATION. The default configuration of the CTC2 is R42 is installed and R43 is unpopulated. This results in the SAA circuitry routed to pin 149 of the DIMM connector. The default configuration was chosen based on early JEDEC documentation. Recent documentation indicates SAA is located on pin 148. Therefore, it is recommend to check the pinout of the device under test and determine if this setting should be changed.



R42/R43 location on the backside of the CTC2 board.

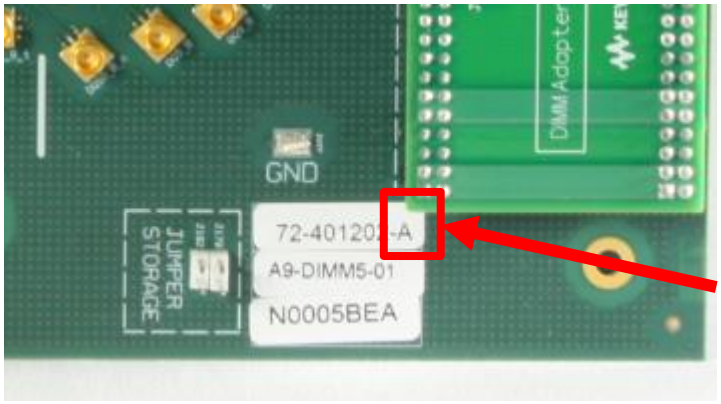
6 Reset Circuit

A pullup resistor, R35, is available on the CTC2 to pullup Reset to 1.1V.

On assembly revisions A through E of the CTC2 board, R35 is unpopulated and it is recommended to populate R35 with a 2.0k resistor. R35 is located near the SMP connector for RESET_n.

Starting on assembly revision F, R35 is populated with a 2.0k resistor and no further action is needed.

The assembly revision is located on a label on the board. It is the last letter at the end of the 72-40120x part number.



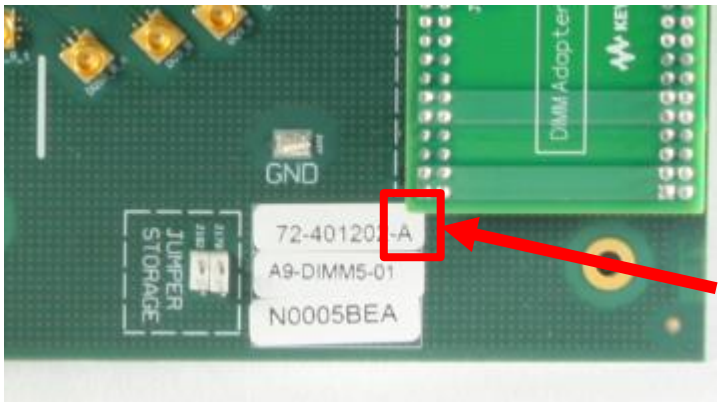
7 GPIO

Four GPIO signals were added to the CTC2 board starting with assembly revision E.

Unfortunately, the GPIO signals did not prove to be useful due to the limited number of them (only 4) and that they are open-drain (drive low and pull high) outputs.

The Reset Automation kit provides many more signals and can be used to drive signals high and low.

The assembly revision is located on a label on the board. It is the last letter at the end of the 72-40120x part number.



8 Calibration Traces

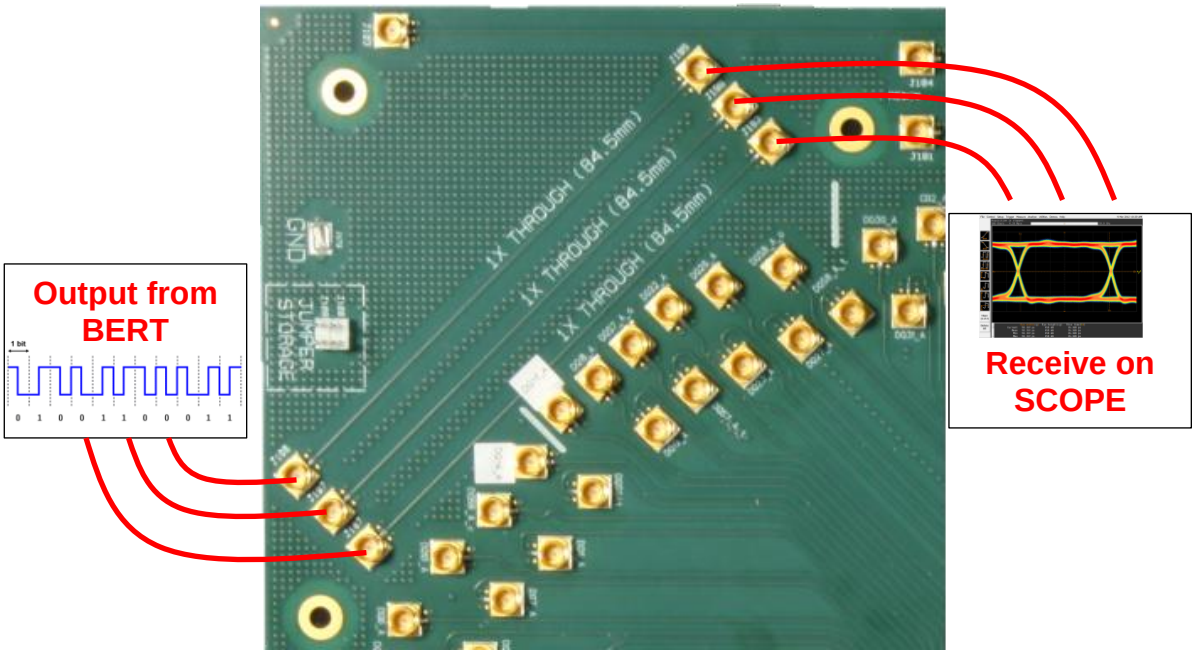
There are three types of calibration structures on the CTC2

- 1X THRU (3 structures)
- 2X THRU
- Open / Short / Load

1X THRU

The 1X THRU calibration structures are used when calibrating and configuring a BERT. The three connections allow calibration of one DQ and one DQS pair at the same time.

A typical calibration setup is shown below.



The 1X THRU trace is the same length as the traces from the DIMM connector to the SMP connectors. Therefore, this calibration structure allows the user to “view” the signal as observed at the DIMM connector location rather than at the SMP on the CTC2. This allows for better calibration of the signal from the BERT because the effects of losses on the CTC2 PCB can be accounted for. A more accurate measurement can then be made.

Additional techniques such as embedded the effects of a DIMM card can be used to move the reference point even closer to the ball of the BGA component.

2X THRU

The 2X THRU calibration structure is used to generate a s-parameter of a trace on the CTC2. The 2X THRU structure is measured and then divided in half. This results in an s-parameter with one SMP and one length of signal trace. The s-parameter can then be used for de-embedded on a scope or similar equipment.

Open / Short / Load

The CTC2 provides an open, short, and load (50-ohm) structure on the board as a traditional calibration method for a VNA. The structures were includes as a back-up calibration method in case the 1X THRU or 2X THRU structures did not work.

9 Ordering Information

The following part numbers may be ordered from Astek. Contact Astek representative for quoting and availability.

Part Number	Description
A9-CTC2-01	DDR5 CTC2 with high-performance socket installed
A9-CTC2-02	DDR5 CTC2 with standard socket installed
A9-CTC2-03	DDR5 CTC2 with NO socket installed
A9-AUTO-01	Reset Automation Kit. Includes GPIO cable

Additional products related to the CTC2 available from Astek.

Part Number	Description
A9-DIMM-01	DDR5 Parametric Test Card
A9-CNTL-01	DDR5 Controller Board w/ RCD and Reset Automation
A9-DBVC-01	DDR5 Data Buffer (DB) Test Card
A9-RCD-01	DDR5 Registering Clock Driver (RCD) Test Card
A9-CMBO-01	DDR5 Combination Test Card
A9-A2PCBL-1000	SMA to SMP cable, 1.0m
A9-A2PCBL-1000P	SMA to SMP cable, 1.0m, matched pair
A9-A2PCBL-0500	SMP to SMP cable, 0.5m
A9-A2PCBL-0500P	SMP to SMP cable, 0.5m, matched pair

10 How to Contact Astek Corporation

Astek Corporation may be contacted by the following methods:

PHONE: (719) 260-1625 (USA)

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