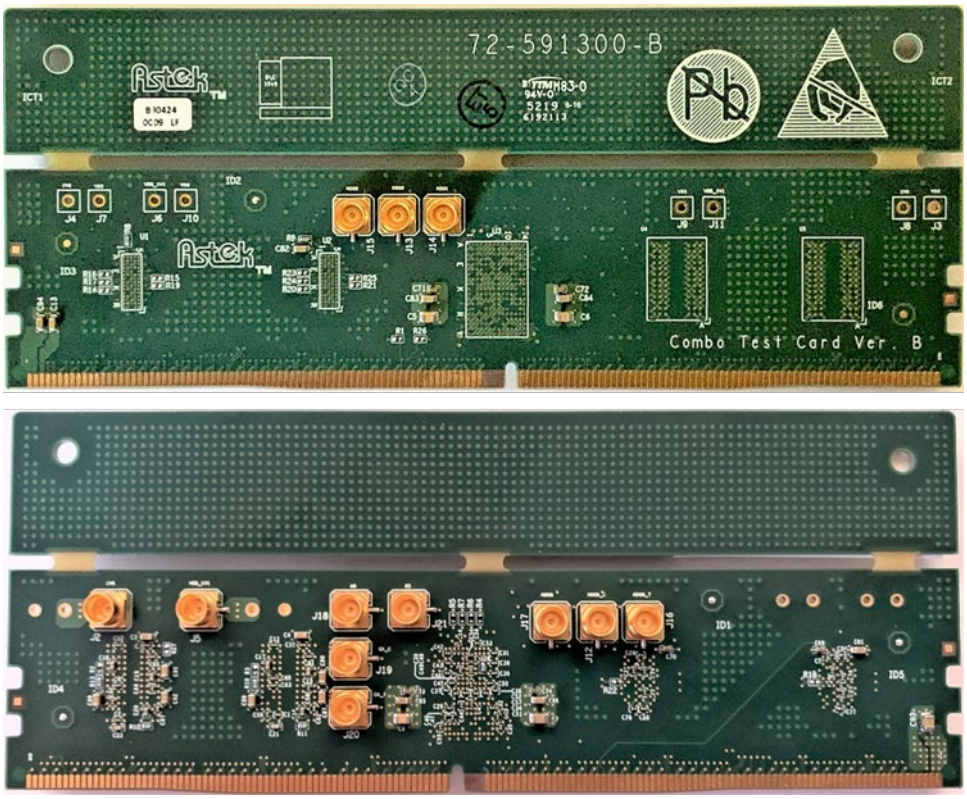
A9-CMBO

User Manual

Transforming Technology into Customer Value

Version: May 27, 2022



1 Introduction / Overview

DDR5 X8 CMBO TEST CARD

A versatile DIMM test card with focus on receiver equalization and loopback BER testing. Including replica channels for calibration of stressed eyes. Data Buffer and DRAM can be configured by either RCD, signals from CTC2 or mother board. Compatible with Astek's A9-CTC2, Channel Test Card.

Features

- RCD interfaced to DRAM and Data Buffer
- Stand-alone
  - Data Buffer
  - Memory

Configuration

- All critical passive Rs and Cs installed
- SMPs installed
- RCD, Memories, and Data Buffers must be provided by customer.

2 Operating CMBO Card

Before Powering On

- Turn Power Supplies OFF
- Remove USB Connector from CTC2
- Insert CMBO Card into CTC2 DIMM connector completely before applying power

Before Removing CMBO Card

- Turn Power Supplies OFF
- Remove USB Connector from CTC2

3 Pin Out Definition

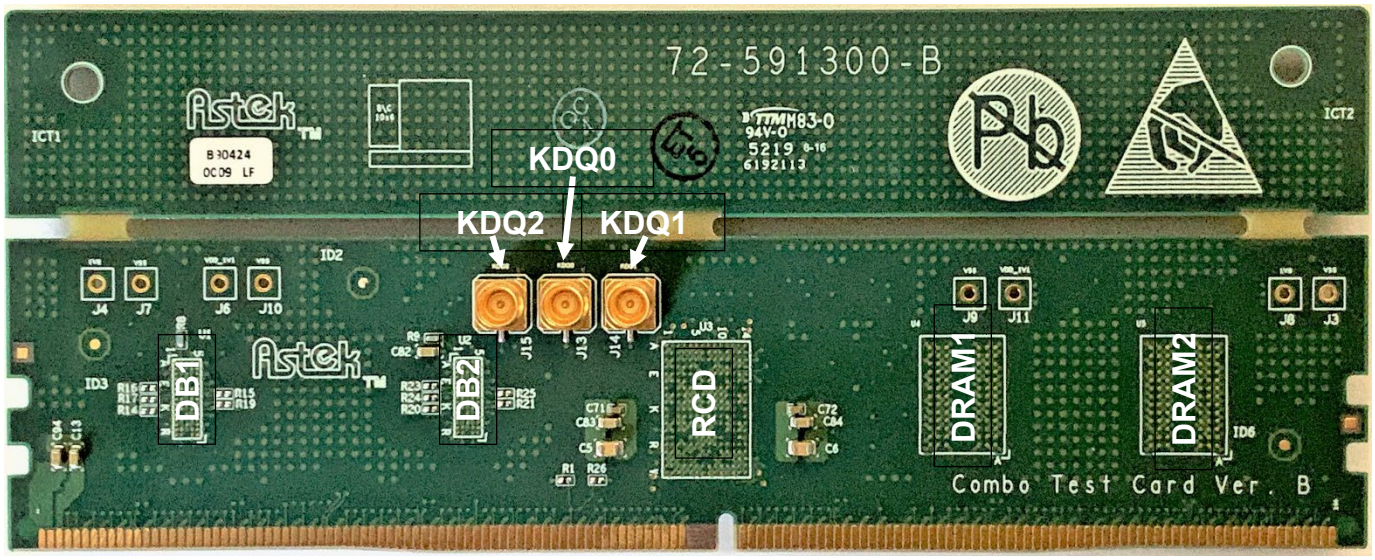


Figure 1: CMBO Card Front

CTC2	DIMM	Signal	Test Points	SMP
Gnd	6, 8, . . .	VSS	J3	
1.8*	3	VDD 1V8	J4	
1.1*	1	VDD	J6	
Gnd	6, 8, . . .	VSS	J7	
1.8*	3	VDD 1V8	J8	
Gnd	6, 8, . . .	VSS	J9	
Gnd	6, 8, . . .	VSS	J10	
1.1*	1	VDD	J11	
CB4_A	58	KDQ0		J13
CB5_A	60	KDQ1		J14
DQS9_A_t	201	KDQ2		J15

* Supply voltages provided by external power supply

Table 1: Top CTC2 Connections, Test Points and SMP's

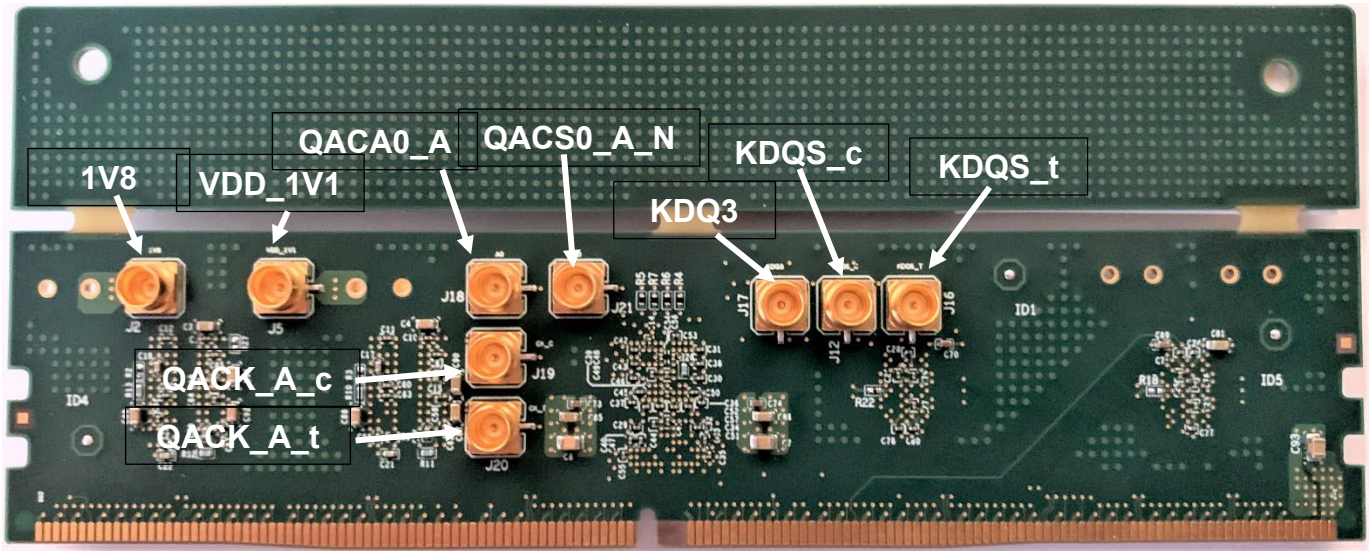


Figure 2: CMBO Card Back

CTC2	DIMM	RCD	Signal	SMP
1.8 V*	3		VDD_1V8	J2
1.1 V*	1		VDD_1V1	J5
DQS4_A_c	56		KDQS_c	J12
DQS4_A_t	55		KDQS_t	J16
CB6_A	203		KDQ3	J17
		QACA0_A (M3)	Test_QACA0_A	J18
		QACK_A_c (M5)	Test_QACK_A_c	J19
		QACK_A_t (M6)	Test_QACK_A_t	J20
		QACS0_A_N (N1)	Test_ QACS0_A_N	J21

Table 2: CTC2 connections and SMP's

DRAM #1 connected to RCD and DIMM contacts for RCD/DRAM Test

Pin	Signal	DIMM Pin	RCD Pin		CTC2
E7	DQ7_B	254	-		DQ7_B
E3	DQ6_B	252	-		DQ6_B
E8	DQ5_B	109	-		DQ5_B
E2	DQ4_B	107	-		DQ4_B
B7	DQ3_B	247	-		DQ4_B
B3	DQ2_B	245	-		DQ2_B
C8	DQ1_B	102	-		DQ1_B
C2	DQ0_B	100	-		DQ0_B
C3	DQS0_B_t	104	-		DQS0_B_t
D3	DQS0_B_c	105	-		DQS0_B_c
C7	DQS1_B_t	249	-		DQS5_B_c
D7	DQS1_B_c	205	-		CB7_A
M7	QBCA13_B	-	A11		
M3	QBCA12_B	-	A9		
M8	QBCA11_B	-	A10		
M2	QBCA10_B	-	A8		
L7	QBCA9_B	-	B12		
L3	QBCA8_B	-	C12		
K8	QBCA7_B	-	A13		
K2	QBCA6_B	-	C14		
J8	QBCA5_B	-	D14		
J2	QBCA4_B	-	E12		
K7	QBCA3_B	-	A12		
K3	QBCA2_B	-	D12		
J7	QBCA1_B	-	B14		
J3	QBCA0_B	-	E14		
G7	QBCK_B_T	-	E9		
H7	QBCK_B_C	-	E10		
H3	QBCS_B_N	-	F14		
M1	CAI	-	-	VDD	
G1	CA_ODT	-	-	PULLUP	
M9	QRST_B_N	-	T10		
G2	MIR	-	-	VSS	
H1	ALERT_N0	236	H1	PULLUP	CB3_B
G9	TEN	-	-	VSS	
A1	LBDQ0	96	-		CB4_B
A9	LBDQS0	98	-		CB5_B

DRAM #2 connected to DIMM contacts (only) for DRAM Test

Pin	Signal	DIMM Pin		CTC2
E7	DQ23_B	276		DQ23_B
E3	DQ22_B	274		DQ22_B
E8	DQ21_B	131		DQ21_B
E2	DQ20_B	129		DQ20_B
B7	DQ19_B	269		DQ19_B
B3	DQ18_B	267		DQ18_B
C8	DQ17_B	124		DQ17_B
C2	DQ16_B	122		DQ16_B
C3	DQS2_B_t	126		DQS2_B_t
D3	DQS2_B_c	127		DQS2_B_c
C7	DQS3_B_t	271		DQS7_B_c
D7	DQS3_B_c	272		DQS7_B_t
M7	CA13	142		DQ29_B
M3	CA12	111		DQ8_B
M8	CA11	285		DQ30_B
M2	CA10	115		DQS1_B_t
L7	CA9	140		DQ28_B
L3	CA8	113		DQ9_B
K8	CA7	280		DQ27_B
K2	CA6	263		DQ14_B
J8	CA5	278		DQ26_B
J2	CA4	265		DQ15_B
K7	CA3	135		DQ25_B
K3	CA2	118		DQ12_B
J7	CA1	133		DQ24_B
J3	CA0	120		DQ13_B
G7	CK1_t	137		DQS3_B_t
H7	CK1_c	138		DQS3_B_c
H3	CS_n	261		DQS6_B_t
M1	CAI	-	VSS	
G1	CA_ODT	-	PULLUP	
M9	RESET_N1	282		DQS8_B_c
G2	MIR	-	VSS	
H1	ALERT_N1	283	PULLUP	
G9	TEN	-	VSS	
A1	LBDQ2	256		DQ10_B
A9	LBDQS2	258		DQ11_B

Table 3: DRAM 1 & DRAM 2 signals to CTC2 SMP connector mapping

Data Buffer #1 connected to DIMM contacts (only) for Data Buffer Test

Signal	Pin	DIMM Pin	CTC2	
DQ7_A	A1	7	DQ0_A	
DQ6_A	C1	9	DQ1_A	
DQ5_A	B1	152	DQ2_A	
DQ4_A	D1	154	DQ3_A	
DQ3_A	M1	14	DQ4_A	
DQ2_A	P1	16	DQ5_A	
DQ1_A	N1	159	DQ6_A	
DQ0_A	R1	161	DQ7_A	
DQS0_A_t	L1	157	DQS5_A_t	
DQS0_A_c	K1	156	DQS5_A_c	
DQS1_A_t	E1	11	DQS0_A_t	
DQS1_A_c	F1	12	DQS0_A_c	
MDQ7_A	A5	172	DQ15_A	
MDQ6_A	C5	170	DQ14_A	
MDQ5_A	B5	27	DQ13_A	
MDQ4_A	D5	25	DQ12_A	
MDQ3_A	M5	165	DQ11_A	
MDQ2_A	P5	163	DQ10_A	
MDQ1_A	N5	20	DQ9_A	
MDQ0_A	R5	18	DQ8_A	
MDQS0_A_t	L5	22	DQS1_A_t	
MDQS0_A_c	K5	23	DQS1_A_c	
MDQS1_A_t	E5	168	DQS6_A_t	
MDQS1_A_c	F5	167	DQS6_A_c	
BCOM2_A	J5	174	DQ18_A	PULLUP
BCOM1_A	H5	31	DQ17_A	PULLUP
BCOM0_A	G5	176	DQ19_A	PULLUP
BCS_N	J1	29	DQ16_A	PULLUP
BCK_A_t	H1	178	DQS7_A_c	PULLUP
BCK_A_c	G1	179	DQS7_A_t	PULLUP
BRST_N	A4	200	DQS9_A_c	
LBTX_DQ0	R4	36	DQ20_A	
LBTX_DQS0	R2	181	DQ22_A	

Data Buffer #2 connected to DIMM contacts and RCD for DB/RCD Test

Signal	Pin	DIMM Pin	RCD Pin	CTC2	
DQ23_A	A1	40	-	DQ24_A	
DQ22_A	C1	42	-	DQ25_A	
DQ21_A	B1	185	-	DQ26_A	
DQ20_A	D1	187	-	DQ27_A	
DQ19_A	M1	47	-	DQ28_A	
DQ18_A	P1	49	-	DQ29_A	
DQ17_A	N1	192	-	DQ30_A	
DQ16_A	R1	194	-	DQ31_A	
DQS2_A_t	L1	190	-	DQS8_A_t	
DQS2_A_c	K1	189	-	DQS8_A_c	
DQS3_A_t	E1	44	-	DQS3_A_t	
DQS3_A_c	F1	45	-	DQS3_A_c	
MDQ23_A	A5	-	-		
MDQ22_A	C5	-	-		
MDQ21_A	B5	-	-		
MDQ20_A	D5	-	-		
MDQ19_A	M5	183	-	DQ23_A	
MDQ18_A	P5	38	-	DQ21_A	
MDQ17_A	N5	-	-		
MDQ16_A	R5	-	-		
MDQS2_A_t	L5	33	-	DQS2_A_t	
MDQS2_A_c	K5	34	-	DQS2_A_c	
MDQS3_A_t	E5	-	-		
MDQS3_A_c	F5	-	-		
BCOM2_A_R	J5	-	R3		PULLUP
BCOM1_A_R	H5	-	R2		PULLUP
BCOM0_A_R	G5	-	T1		PULLUP
BCS_N_R	J1	-	R1		PULLUP
BCK_A_t_R	H1	-	R6		PULLUP
BCK_A_c_R	G1	-	R5		PULLUP
BRST_N_R	A4	-	R4		
LBTX_DQ1	R4	51	-	CB0_A	
LBTX_DQS1	R2	196	-	CB2_A	

Table 4: Data Buffer 1 & Data Buffer 2 signals to CTC2 SMP connector mapping

RCD

RCD to DIMM contacts

Pin	Signal	DIMM pin	CTC2
U6	ALERT_N	62	ALERT_n
U1	CA0_A	66	CA0_A
W8	CA0_B	78	CA0_B
V1	CA1_A	211	CA1_A
V9	CA1_B	223	CA1_B
W2	CA2_A	68	CA2_A
W10	CA2_B	80	CA2_B
V3	CA3_A	213	CA3_A
V11	CA3_B	225	CA3_B
W4	CA4_A	70	CA4_A
W12	CA4_B	82	CA4_B
W6	CA5_A	215	CA5_A
W13	CA5_B	227	CA5_B
V7	CA6_A	72	CA6_A
V14	CA6_B	84	CA6_B
T8	CK_c	218	CK_c
T7	CK_t	217	CK_t
U3	CS0_A_N	64	CS0_A_n
T11	CS0_B_N	76	CS0_B_n
T4	CS1_A_N	209	CS1_A_n
U12	CS1_B_N	221	CS1_B_n
V5	PAR_A	74	PAR_A
U14	PAR_B	229	PAR_B
H5	QECK_A_c	87	LBS/RSP_B_n
H6	QECK_A_t	86	BD/RSP_A_n
H10	QECK_B_c	231	RFU_4
H9	QECK_B_t	232	RFU_5
P7	QLBD	53	CB1_A
P8	QLBS	198	CB3_A
U9	RESET_n	207	RESET_n

Table 5: RCD signals to CTC2 SMP connector mapping

4 Ordering Information

The following part numbers may be ordered from Astek. Contact Astek for quoting and availability.

Part Number	Description
A9-CTC2-01	DDR5 CTC2 with high-performance socket installed
A9-CTC2-02	DDR5 CTC2 with standard socket installed
A9-CTC2-03	DDR5 CTC2 with NO socket installed
A9-AUTO-01	Reset Automation Kit. Includes GPIO cable

Additional products related to the CTC2 available from Astek.

Part Number	Description
A9-DIMM-01	DDR5 Parametric Test Card
A9-CNTL-01	DDR5 Controller Board w/ RCD
A9-RCD-01	DDR5 Registering Clock Driver (RCD) Test Card
A9-CMBO-01	DDR5 Combination Test Card
A9-A2PCBL-1000	SMA to SMP cable, 1.0m
A9-A2PCBL-1000P	SMA to SMP cable, 1.0m, matched pair
A9-A2PCBL-0500	SMP to SMP cable, 0.5m
A9-A2PCBL-0500P	SMP to SMP cable, 0.5m, matched pair

5 How to Contact Astek Corporation

Astek Corporation may be contacted by the following methods:

PHONE: (719) 260-1625 (USA)

FAX: (719) 260-1668 (USA)

EMAIL: support@astekcorp.com

WEBSITE: www.astekcorp.com

