# A9-CKD-01

DDR5 Clock Driver SI Test Card

Transforming Technology into Customer Value

## User Guide

**Version: April 8, 2025**

# 1 Introduction / Overview

## DDR5 Clock Driver Test Card

A versatile DIMM test card focused on Clock Driver Signal Integrity (SI) measurement. It Minimizes signal integrity impact by using JEDEC reference load termination in combination with minimal trace lengths. Provides high impedance oscilloscope probing access to Tx and Rx outputs of the Clock Driver under test. Clock Driver SI test cards are compatible with Astek's A9-CTC2.

## Features

- Clock Driver test points compatible with Keysight MX0100 high performance oscilloscope probes
- Minimizes SI impact using JEDEC reference load termination.

## Test Measurements

- Jitter
- Idd
- $t_{STAOFF}/t_{DYNOFF}$
- Ron
- Slew Rate
- Vox

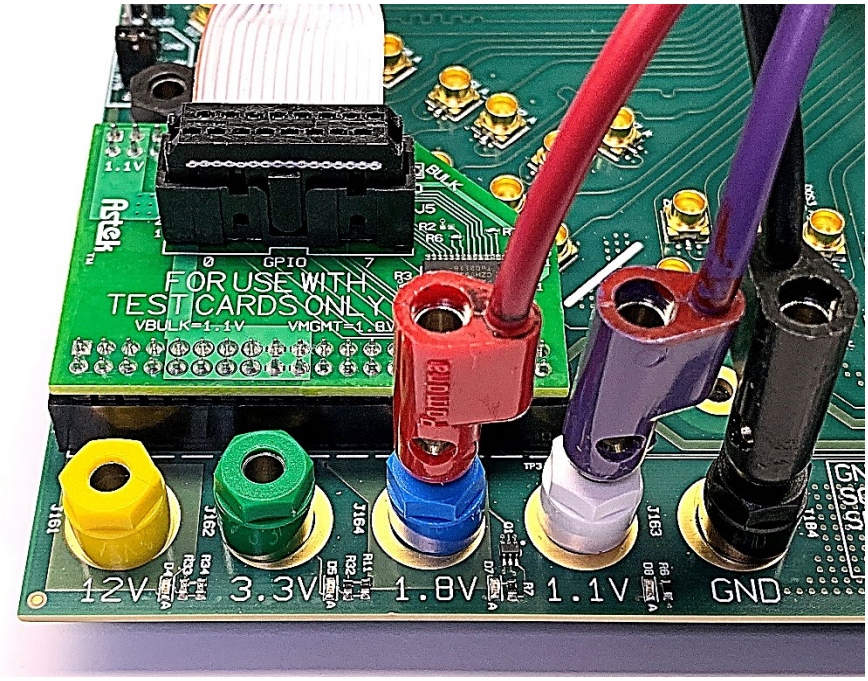
## Configuration

- All critical passive Rs and Cs installed.
- Clock Drivers provided by customer.

# 2 CTC2 - Clock Driver Card Set Up

## Set Up

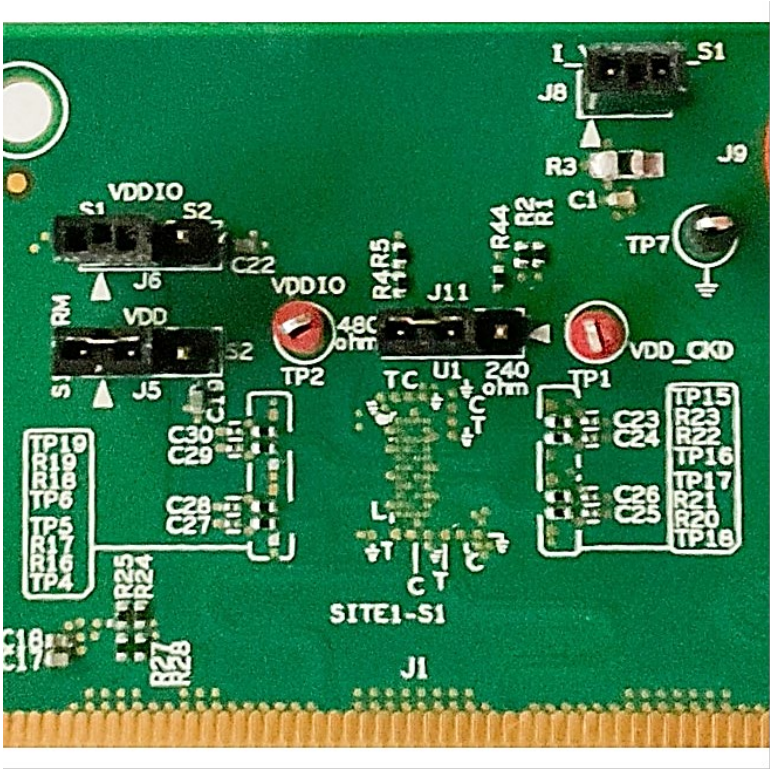
- Connect USB Cable to CTC2




- Install Test Card Power Module

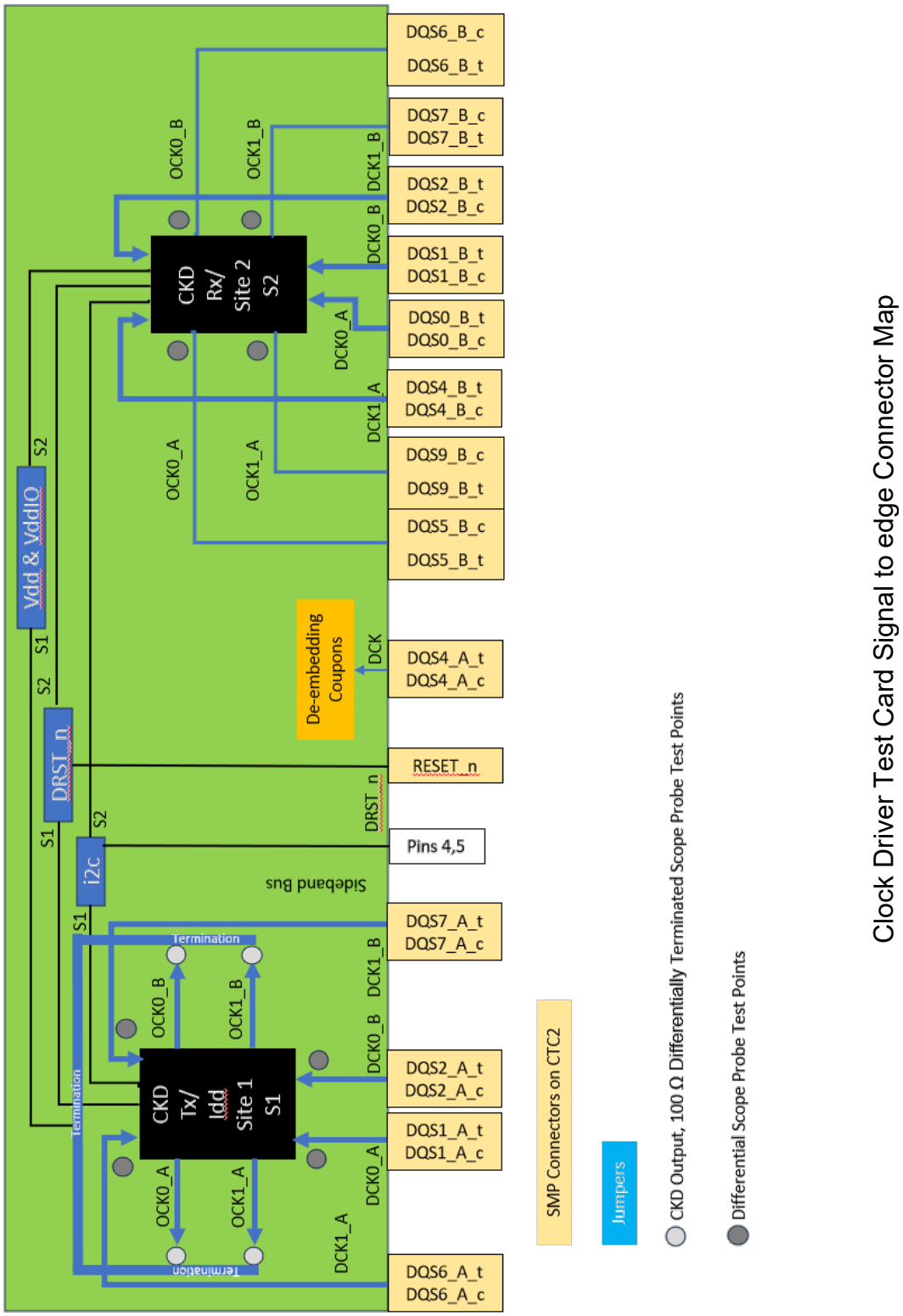
- Attach 1.1 V and 1.8 V power supplies to CTC2

- Site 1- S1 Vdd Power - Device S1's Vdd is powered from binding posts J9 and J10
- Site 1 Clock Driver's, QCK[1:0]_t/c termination voltage is provided by the CTC2's 1.1 V supply through jumper J5, S1 (see photo below)
- Site 2 Clock Driver's, Vdd is supplied the CTC2's 1.1 V supply when jumper J5 is in position S2 (see photo below)

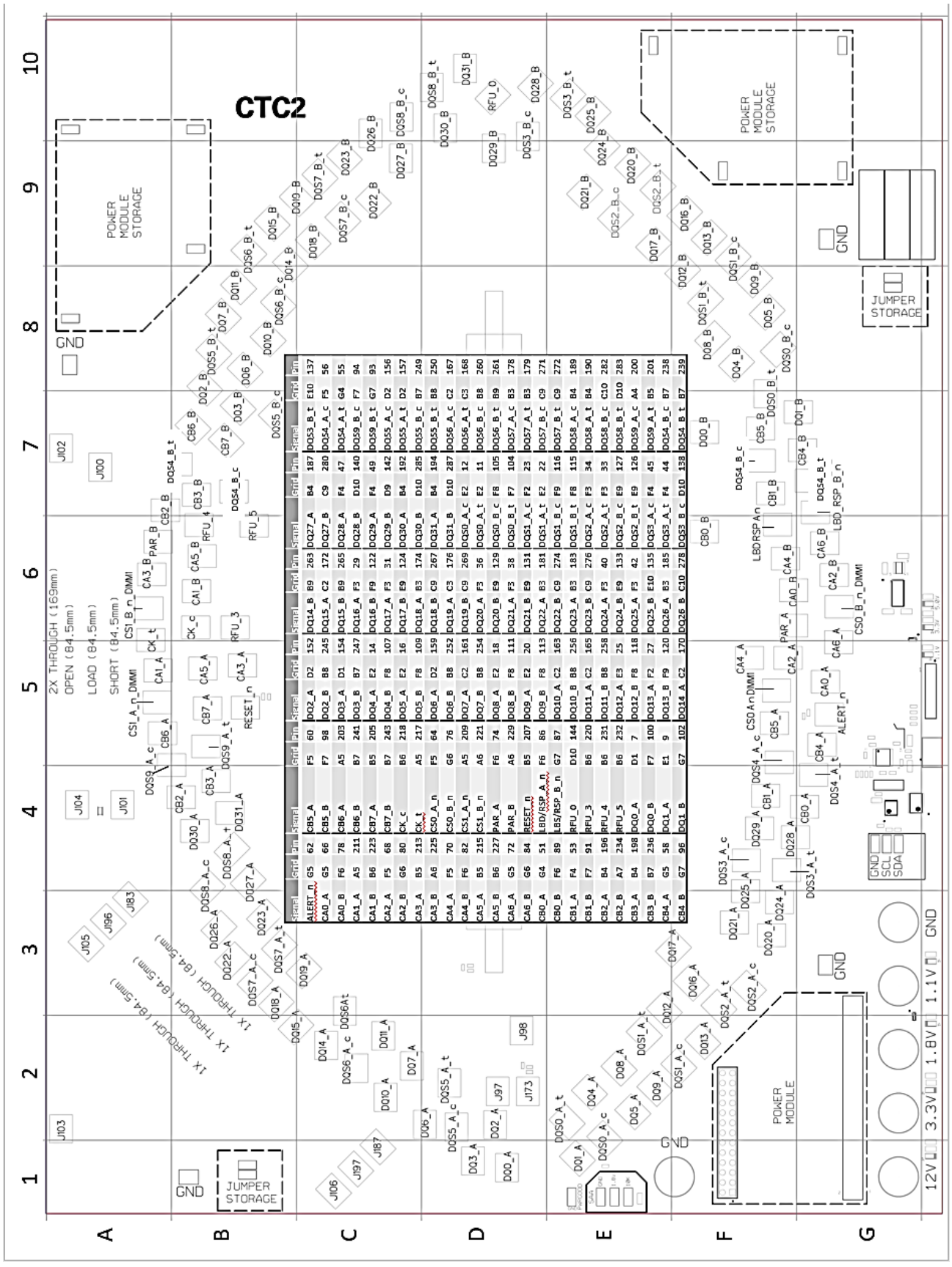



- Connect Reset Automation Cable (A9-AUTO-01) RST_n lead to CTC2 RESET_n SMP connector
- Clock Drive Sites S1 and S2 are clocked separately. See "Clock Driver Signal to CTC2 SMP Mapping" to identify Site S1 and S2 input and output signal locations (CTC2, SMP).

# 3 Clock Driver Signal to CTC2 SMP Mapping




Clock Driver Test Card Signal to edge Connector Map




CTC2 Signal - SMP Map

# 4 Clock Driver Test Card Set Up

## Jumper Assignment

### Place Jumpers to activate Clock Driver IC under test

- Install Jumpers J2, J3, J4, J5, J6 in position Site 1 (S1) to select Clock Driver located at left end card.
- Correspondingly installing Jumpers J2, J3, J4, J5, J6 in position Site 2 (S2) selects Clock Driver located at right end.

| REF DES | SITE1 | SITE 2 | DESC |
|---|---|---|---|
| J2 | 1/2 | 2/3 | RESET |
| J3 | 1/2 | 2/3 | SCL |
| J4 | 1/2 | 2/3 | SDA |
| J5 | 1/2 | 2/3 | VDD |
| J6 | 1/2 | 2/3 | VDD_IO |

### ZQ Calibration

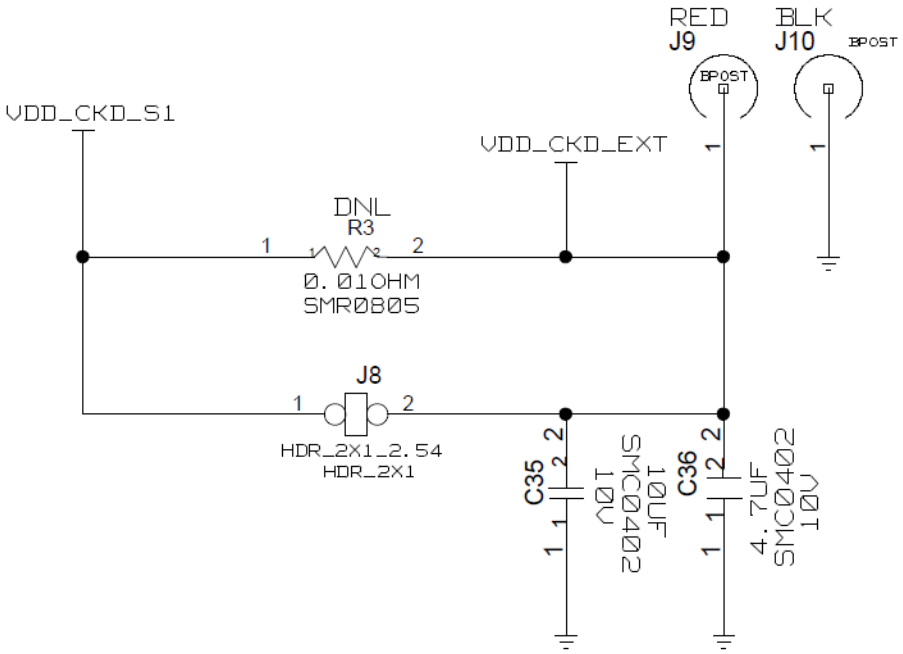
- Jumpers J11 and J12 provide the means of selecting the ZQ CAL resistor value Site 1 (J11) and Site 2 (J12)

| ZQCAL | | | |
|---|---|---|---|
| | 240Ω | 480Ω | |
| J11 | 1/2 | 2/3 | SITE 1 |
| J12 | 1/2 | 2/3 | SITE 2 |

# Idd Current

**Site S1, Idd is measured by.**

- removing jumpers J8
- measure voltage drop across R3, J8 pins (1 mV ~ 100 mA)



# 5 Clock Driver i2c Control

## Clock Driver initialization

Connect Reset Automation cable, lead RST_n to CTC2, RESET SMP.

Reset
- setgpio off

Enable
- setgpio on

## Writing and Reading Clock Driver Registers

Clock Driver Registers can be Written to and read from using CTC2 Controller Commands over USB

Register Write

- i2cWriteByte <device address> <register> <data>

Example

- i2cWriteByte 5F 00 01

Register Read

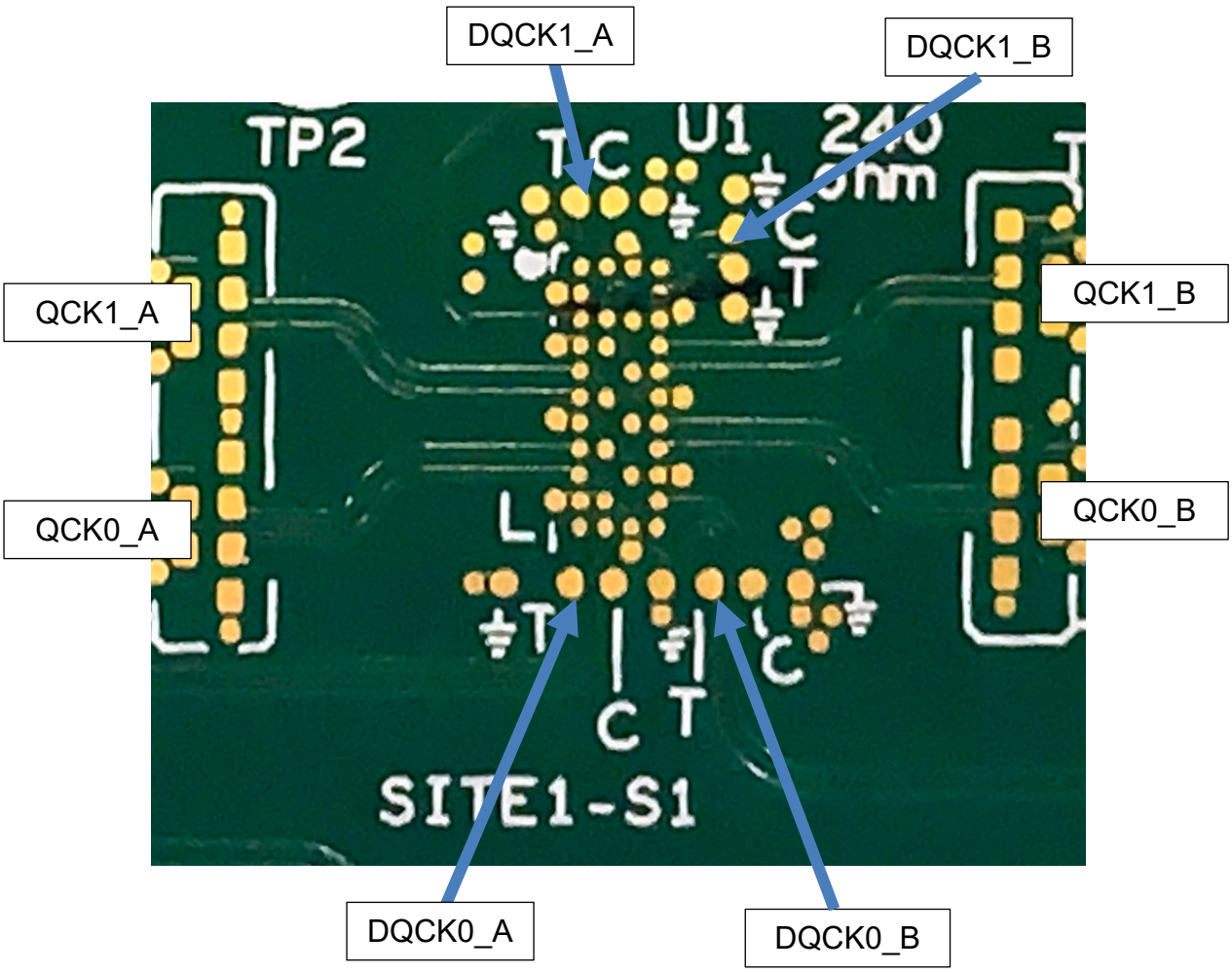
- i2cReadByte <device address> <register>

Example

- i2creadbyte 5F 00
  *value read* 0x00: 0x01

# 6 Scope Test Points

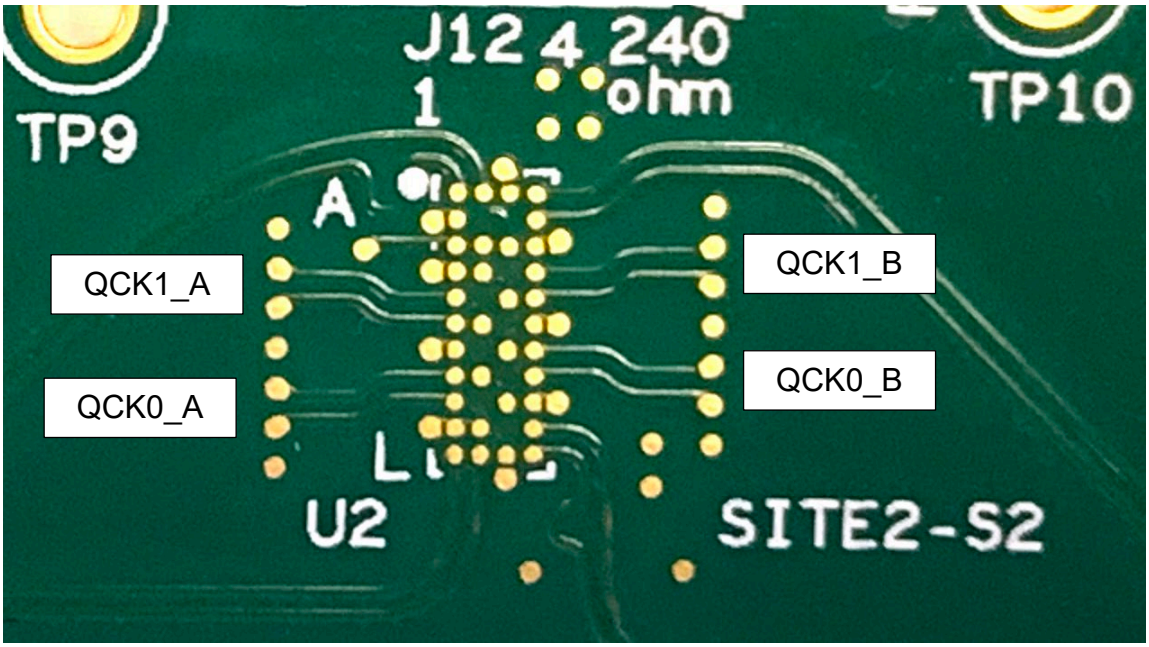
## Site 1 - S1




**Scope Probe Test Points**
*Compatible with Keysight MX0100 differential probe tips*

*Note: all clock signals accessible from Clock Driver board front*

## Site 2 - S2




**Scope Probe Test Points**
*Compatible with Keysight MX0100 differential probe tips*

## Scope Probe De-Embedding Coupon


**Site 2 DCK Scope Probe De-Embedding Coupon**
*Keysight MX0100 differential probe tip shown.*

*Note: all clock signals accessible from Clock Driver board front*

# 7 Ordering Information

The following part numbers can be ordered from Astek. Contact Astek for quoting and availability.

| Part Number | Description |
|---|---|
| A9-CTC2-01 | DDR5 CTC2 with high-performance socket installed |
| A9-AUTO-01 | Reset Automation Kit. Includes GPIO cable |
| A9-CKD-01 | Clock Driver Test Card w/o Clock Drivers |
| | |

Additional products related to the CTC2 are available from Astek.

| Part Number | Description |
|---|---|
| A9-DIMM-01 | DDR5 Parametric Test Card |
| A9-CNTL-01 | DDR5 Controller Board w/ RCD |
| A9-WCNTL-01 | DDR5 Wide Controller w/ RCD |
| A9-RCD-01 | DDR5 Registering Clock Driver (RCD) Test Card |
| A9-CMBO-01 | DDR5 Combo Card |
| A9-X16CMBOx-01 | DDR5 X16 Combo Card |
| A9-UDIMM-01 | UDIMM Riser transition from CTC2 RDIMM to UDIMM |
| A9-SIT-01 | RCD SI Test Card |
| A9-SODIMM-01 | SPDIMM Riser transition from CTC2 RDIMM to SODIMM |
| A9-RPLC-01 | DDR5 Replica Channel |

# 8 How to Contact Astek Corporation

Astek Corporation may be contacted by the following methods:

PHONE: (719) 260-1625 (USA)

FAX: (719) 260-1668 (USA)

EMAIL: support@astekcorp.com

WEBSITE: www.astekcorp.com

*This information in this document is subject to change without notice.*