

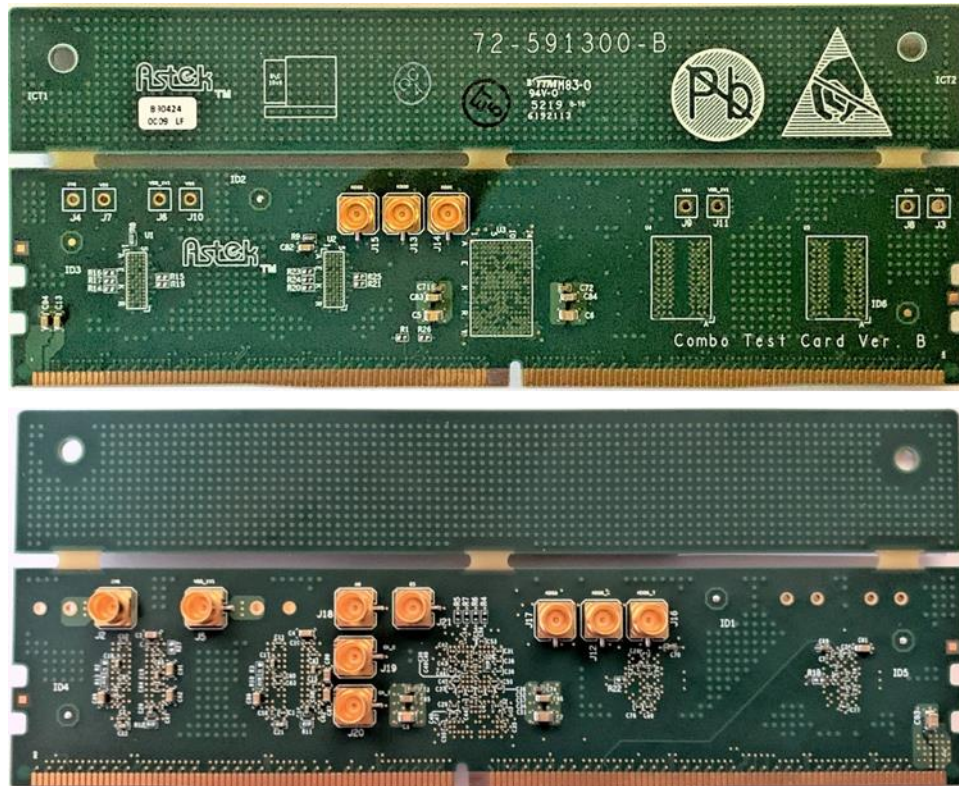


Transforming Technology  
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# A9-COMBO

## Replica Channel Application Note

Version: March 31, 2021



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## DDR5 x8 COMBO TEST CARD

The DDR5 x8 Combo Test Card is a versatile DIMM test card for receiver equalization and loopback BER testing. The Card includes replica channel traces for calibration of stressed eyes. This application note explains the use of the replica traces to calibrate the source when used with the Astek A9-CTC2, DDR5 Channel Test Card.

### CAUTION

Always remove power from the CTC2 before inserting or removing a DIMM.

## Replica Traces

The DDR5 x8 Combo Test Card contains a set of six replica traces:

- KDQS\_T at J16 on the back
- KDQS\_C at J12 on the back
- KDQ3 at J17 on the back
- KDQ2 at J15 on the front
- KDQ1 at J14 on the front
- KDQ0 at J13 on the front

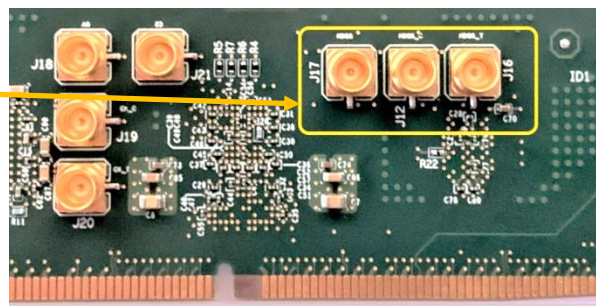


Figure 1 - Back View

The SMP locations are shown in the figures to the right.

The connections on the CTC2 (SMP) and on the Combo Card (SMP) for the replica traces are shown in Table 1 below.

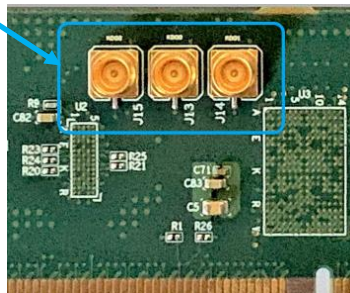


Figure 2 - Front View

Table 1 - CTC2 and Combo Card SMPs

| CTC2     | DIMM | Signal | SMP |
|----------|------|--------|-----|
| CB4_A    | 58   | KDQ0   | J13 |
| CB5_A    | 60   | KDQ1   | J14 |
| DQS9_A_t | 201  | KDQ2   | J15 |
| CB6_A    | 203  | KDQ3   | J17 |
| DQS4_A_c | 56   | KDQS_C | J12 |
| DQS4_A_t | 55   | KDQS_T | J16 |

## Calibration

The intended use for the replica traces is to attach a BERT and a scope, as shown in the block diagram in Figure 3. The BERT can be adjusted to achieve the desired Eye at the Combo Card for testing the DDR5 chip receiver. When the desired Eye is seen at the KDQ\* SMP connector, move the BERT cable from the calibration path SMP connector on the CTC2 to the CTC2 SMP connector for the signal that you want to test.

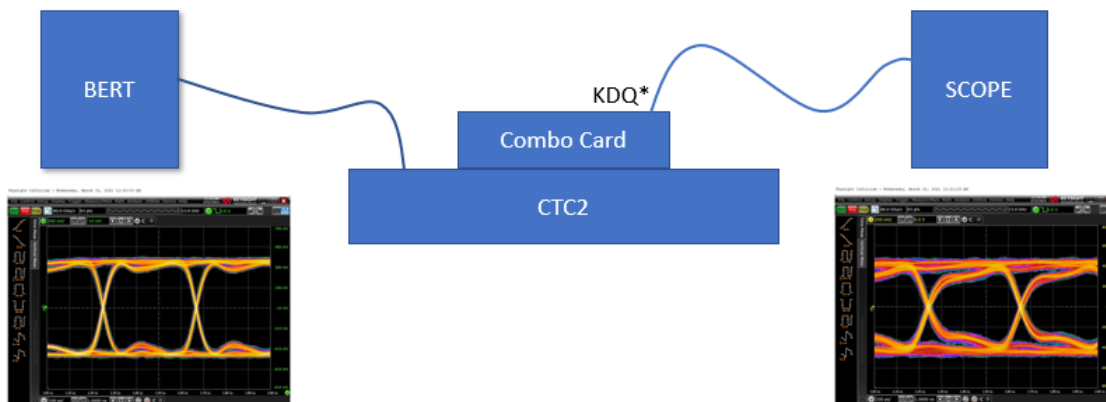
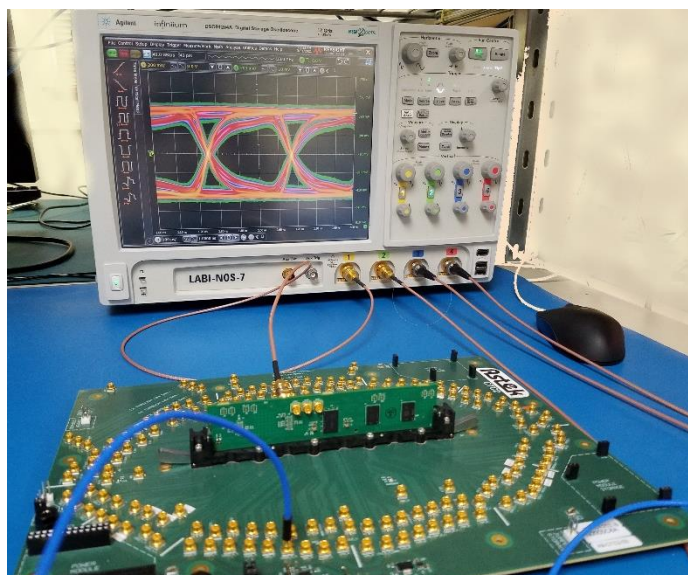


Figure 3 - Calibration Configuration

A proposed procedure to follow is:

- (1) Attach the Signal Source (Bit Error Rate Tester/BERT or Arbitrary Waveform Generator/AWG) to the CTC2 using an SMP cable. Refer to the “CTC2” column in Table 1 to identify the SMP on the CTC2 to attach the cable to.
- (2) Attach a cable from the Combo Card KDQ\* SMP to an Oscilloscope. Refer to Table 1 to identify the SMP on the Combo Card that corresponds to the CTC2 signal path that was used in step (1) above.
- (3) Adjust the Signal Source until the signal displayed on the Scope matches the signal characteristics that you want at the BGA pad of the DDR chip,
- (4) Move the SMP cable on the CTC2 to the desired input for the DDR signal that you would like to test. The setup is shown in the photo below.



Following the steps listed above, you will present a signal to the DUT (the BGA pad on the Combo Card) that matches the signal displayed on the Scope. Depending on how accurate you want the signal characteristics to be, the factors that you need to account for are:

- (1) The losses in the SMP-to-Scope cable
  - a. This can be de-embedded using the Scope InfiniiSim capability to de-embed the cable response
- (2) The difference between the Scope 50 Ohm termination and the termination of the DDR chip on the Combo Card

The different replica traces have different lengths. You should choose which replica trace to use, closely matching the length of the replica trace to the length of the signal to be tested, based on the data in Table 2.

Table 2 - Combo Card Trace Lengths

| Signal   | Trace Length (mm) | Signal   | Trace Length (mm) |
|----------|-------------------|----------|-------------------|
| KDQS_T   | 22.9              | KDQ0     | 22.1              |
| KDQS_C   | 22.9              | KDQ1     | 22.6              |
| KDQ3     | 23.7              | KDQ2     | 22.9              |
| DQS0_A_T | 22.9              | DQS1_A_T | 22.1              |
| DQS0_A_C | 22.9              | DQS1_A_C | 22.1              |
| DQ0_A    | 22.9              | DQ4_A    | 22.9              |
| DQ1_A    | 22.9              | DQ5_A    | 22.9              |
| DQ2_A    | 23.7              | DQ6_A    | 22.1              |
| DQ3_A    | 23.7              | DQ7_A    | 22.1              |
| DQS2_A_T | 22.9              | DQS3_A_T | 22.1              |
| DQS2_A_C | 22.9              | DQS3_A_C | 22.1              |
| DQ16_A   | 22.9              | DQ20_A   | 22.9              |
| DQ17_A   | 22.9              | DQ21_A   | 22.9              |
| DQ18_A   | 23.7              | DQ22_A   | 22.1              |
| DQ19_A   | 23.7              | DQ23_A   | 22.1              |
| DQS0_B_T | 23.7              | DQS1_B_T | 22.9              |
| DQS0_B_C | 23.7              | DQS1_B_C | 22.9              |
| DQ0_B    | 22.6              | DQ4_B    | 23.7              |
| DQ1_B    | 23.7              | DQ5_B    | 22.1              |
| DQ2_B    | 22.9              | DQ6_B    | 22.9              |
| DQ3_B    | 22.9              | DQ7_B    | 22.9              |
| DQS2_B_T | 22.1              | DQS3_B_T | 22.9              |
| DQS2_B_C | 22.1              | DQS3_B_C | 22.9              |
| DQ16_B   | 23.7              | DQ20_B   | 23.7              |
| DQ17_B   | 22.1              | DQ21_B   | 22.6              |
| DQ18_B   | 22.9              | DQ22_B   | 22.9              |
| DQ19_B   | 22.9              | DQ23_B   | 22.9              |



The following items shown in this application note are available from Astek:

- DDR5 x8 Combo Test Card, part number A9-COMBO-01
- DDR5 Compliance Test Card (CTC2), part number A9-CTC2-01

Related products that are available to assist in DDR5 testing:

- DDR5 x16 Combo Test Card, part number A9-X16 COMBO-01
- DDR5 RDIMM Parametric Test Card, part number A9-DIMM5-01
- DDR5 Reset Automation Kit, part number A9-AUTO-01
- DDR5 Controller Board, part number A9-CNTRL-01
- DDR5 Wide Controller Board, part number A9-WCNTRL-01
- DDR5 x4/x8 Signal Integrity Interposer, part number A9008-CHR-40

## How to Contact Astek Corporation

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Astek Corporation may be contacted by the following methods:

PHONE: (719) 260-1625 (USA)

FAX: (719) 260-1668 (USA)

EMAIL: [support@astekcorp.com](mailto:support@astekcorp.com)

WEBSITE: [www.astekcorp.com](http://www.astekcorp.com)