DDR5 CTC2 S-Parameter De-Embedding Model

The CTC2 was designed to support DDR5 DIMM testing. The mapping of the signals to I/O ports is shown in Table 1 below.

Table 1 CTC2 Model Port Mapping

Port	Connection
1	SMP
2	DIMM

The traces between the SMP connector and DIMM have been precisely matched to allow the user to utilize a single S2P file to de-embed any of the DDR5 signal paths on the CTC2. The S2P de-embedding model includes:

(1) the SMP connector that is soldered to the CTC2 board,
(2) the trace on the CTC2 board, and
(3) the DDR5 DIMM test socket

S-Parameters

The insertion loss for the model is shown in the following figure. The insertion loss of all DQ signals tracks very well, so this model can be used to de-embed the effects of the CTC2 for all DDR5 signals available on the CTC2.

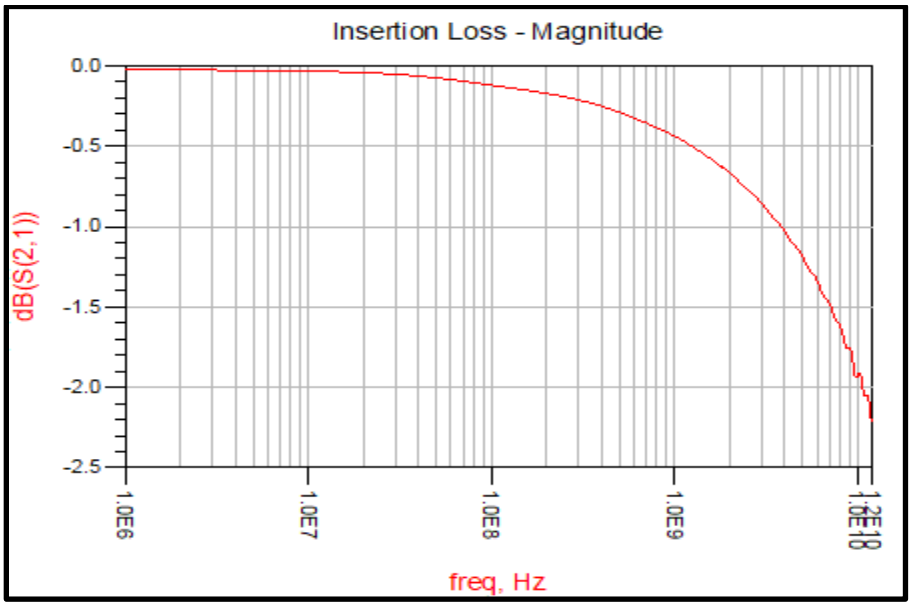

Figure 1 CTC2 Insertion Loss

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