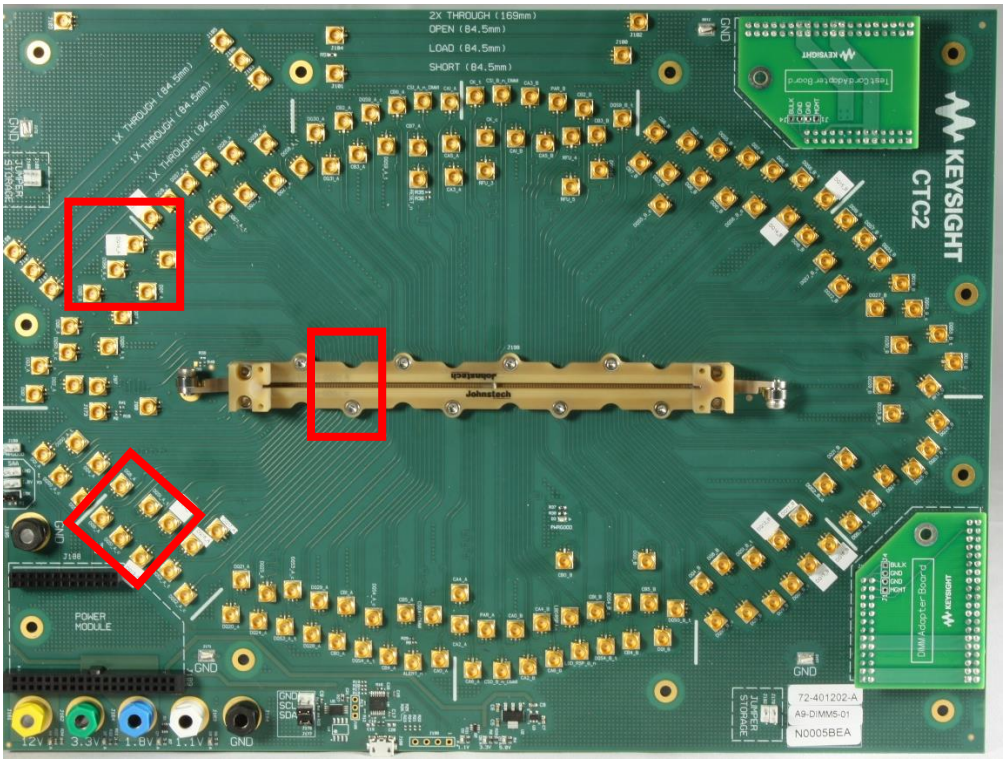
DDR5 CTC2 S-Parameter Simulation Model

The 20-port S-Parameter model includes CTC2 losses and cross-talk to allow the end user to evaluate the expected performance of the CTC2 in their simulation environment for their DDR5 DIMM testing purposes.

A single Byte Lane of signals was extracted for this model. The mapping of the signals to I/O ports is shown in Table 1 below.

Table 1 S-Parameter Model Port Mapping

SMA Port	DIMM Port	DDR5 Signal
1	11	DQ8
2	12	DQ9
3	13	DQ10
4	14	DQ11
5	15	DQ12
6	16	DQ13
7	17	DQ14
8	18	DQ15
9	19	DQS1_t
10	20	DQS1_c



The schematic for the model is shown in Figure 1 below. The ten small S2P block in the left quarter of the schematic are the SMP models. The 20-port model in the center (CTC2_PCB) is the model extracted from the CTC2 board. The 20-port model on the right (DIMM) is the Johnstech 400a Series Contactor.

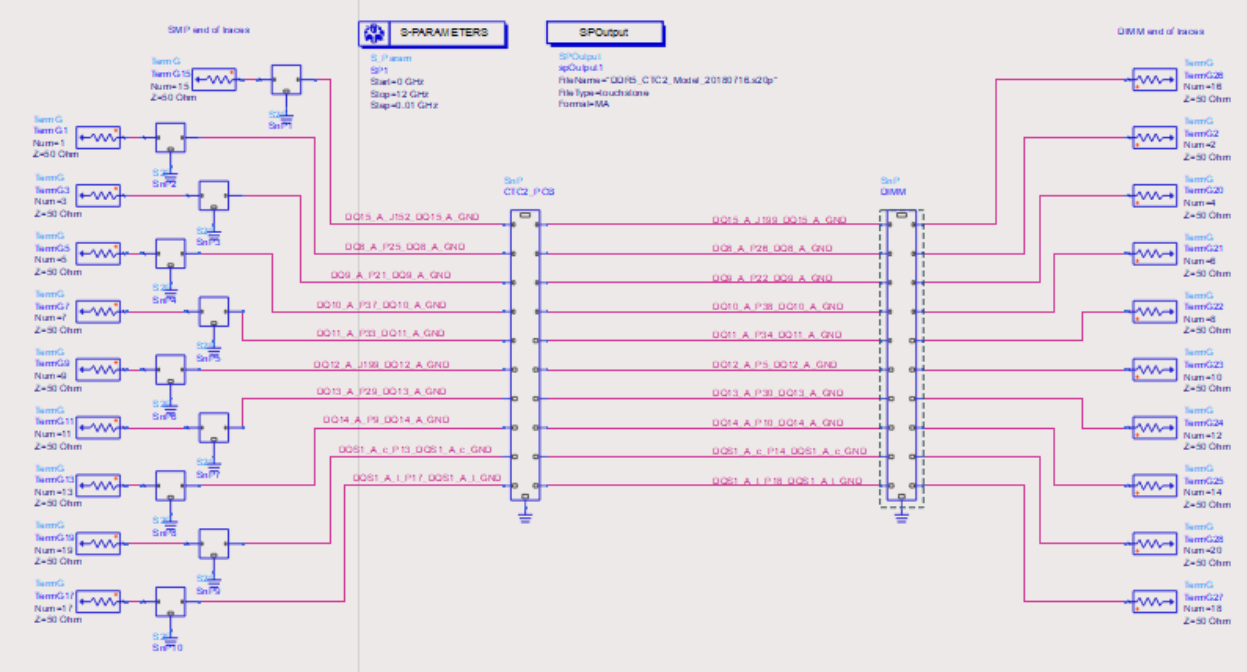


Figure 1 Top Level Model Schematic

The SMP model does not include coaxial cable or the mating connector. The input reference plane (on the left) is at the SMP connector.

The CTC2 model was extracted from the ODB++ artwork used to create the PCB. This model includes system losses and cross-talk.

The DIMM socket model provided by Johnstech includes a short section of trace at all ports. The traces on the CTC2 PCB were adjusted to compensate for the trace segment included in the Johnstech model. The output ports (on the right in Figure 1) include 2.7 mm of 50 Ohm trace on the DIMM, after the Johnstech DIMM socket. If the characteristics of this trace are expected to be significant (e.g. delay), the system simulation must be adjusted to compensate.

S-Parameters

The insertion loss and crosstalk for the modelled signals are shown in the following figures. The insertion loss of all DQ signals tracks very well. The insertion loss for the DQS signals drops off slightly above about 7 GHz.

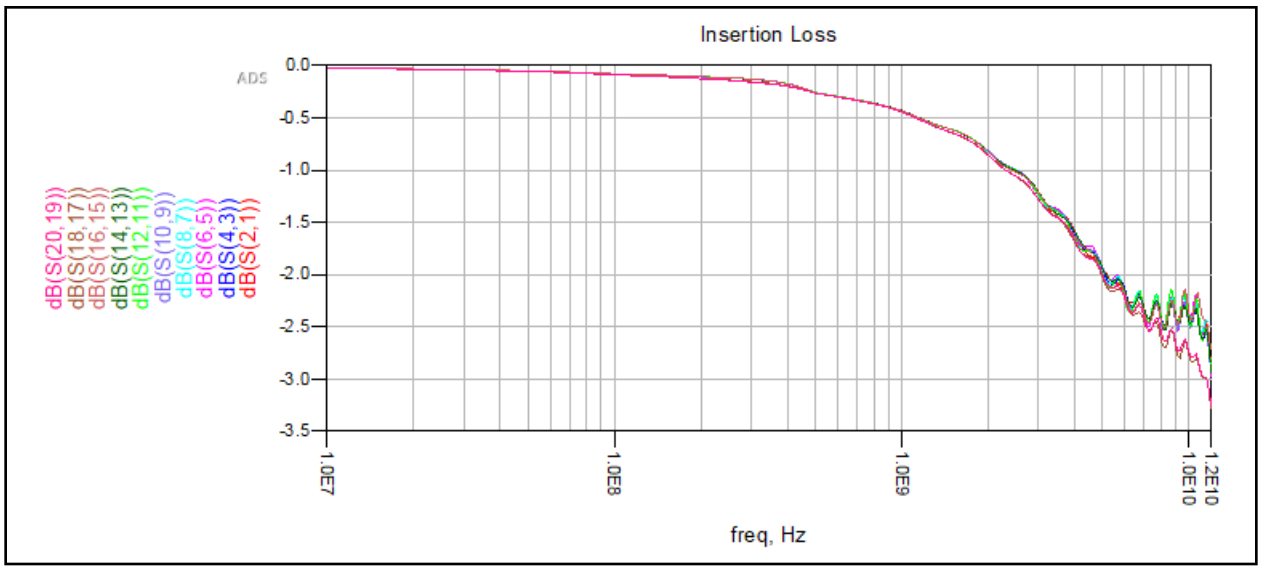


Figure 2 CTC2 Byte Lane 1 Insertion Loss

Crosstalk

Worst case crosstalk on byte lane 1 of the CTC2 is between DQ9 (victim) and DQ8/DQS_t (aggressors). Figure 3 shows the results of the crosstalk simulation for DQ9, the worst-case victim. The small chart on the bottom-left of Figure 3 lists the signals and their corresponding port numbers. Odd ports are the SMP connections. Even ports are on the DIMM.

The m1 marker in the plot is located at 6 GHz and shows the crosstalk values for the coupling between all signals and DQ9 in the upper-right box of Figure 3. (Note that port 4 is the insertion loss for the DQ9 path. This is not included in the crosstalk calculation.) The table near the bottom-right shows the two highest coupling signals (DQ8 and DQS_t) and the sum of their coupling onto the DQ9 DIMM port.

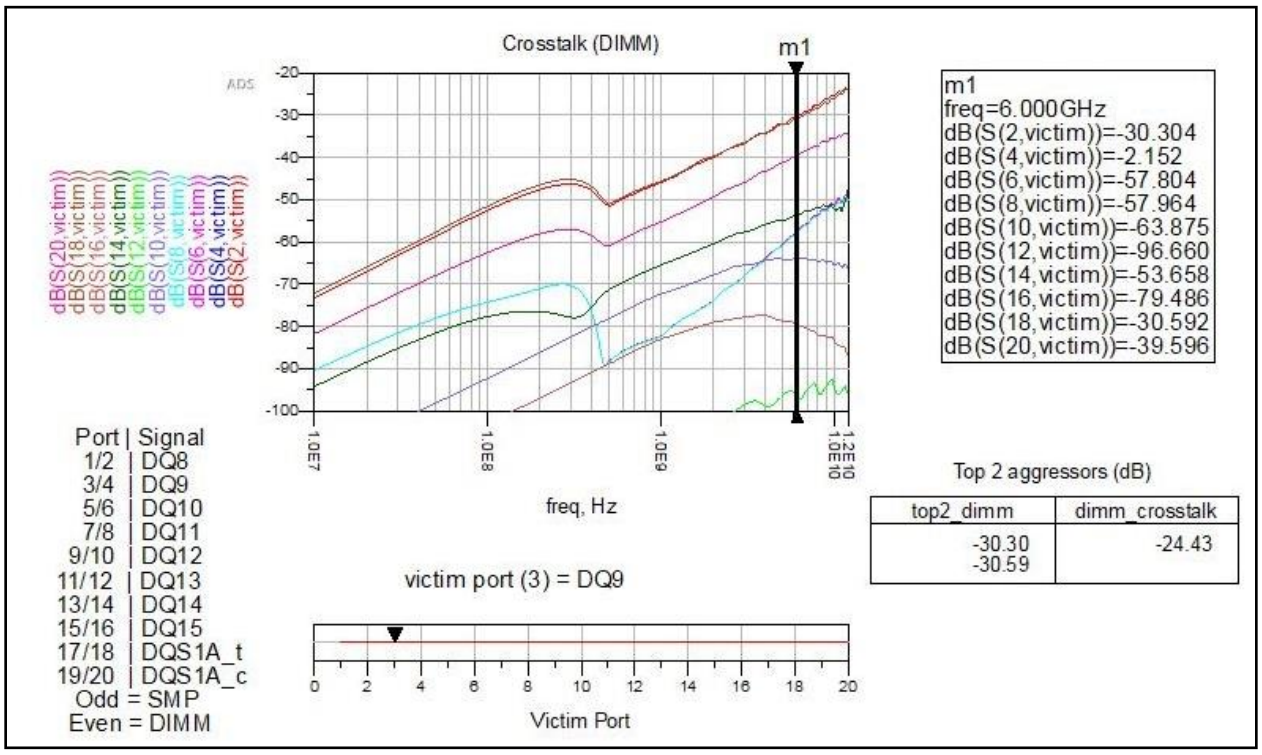


Figure 3 CTC2 Byte Lane 1 Worst Case Crosstalk

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