# Errata for DDR5 RDIMM Parametric Test Fixture

The A9-DIMM5-01 DDR5 RDIMM Parametric Test Fixture (Fixture) was developed prior to the release of the JEDEC standard for the DDR5 RDIMM. In the final release standard document, there were changes that re-arranged some of the signal assignments in the B-channel. These were essentially name changes to the defined signal pins. No power/ground pins changed to signals and no signals changed to power/ground. The Fixture used the signal assignment definition from the pre-release standard in the silk screen labels. The changes are documented in the tables below.

*Table 1. Signal Re-mapping*

| Signal Name | Parametric Test Fixture Pin | Released JEDEC Standard Pin |
|---|---|---|
| CS0_B | 76 | 84 |
| CS1_B | 221 | 229 |
| CA0_B | 78 | 76 |
| CA1_B | 223 | 221 |
| CA2_B | 80 | 78 |
| CA3_B | 225 | 223 |
| CA4_B | 82 | 80 |
| CA5_B | 227 | 225 |
| CA6_B | 84 | 82 |
| PAR_B | 339 | 227 |
| CB0_B | 89 | 96 |
| CB1_B | 91 | 98 |
| CB2_B | 234 | 241 |
| CB3_B | 236 | 243 |
| CB4_B | 96 | 89 |
| CB5_B | 98 | 91 |
| CB6_B | 241 | 234 |
| CB7_B | 243 | 236 |

In order to probe the signal listed in the second column of Table 2, attach your cable to the SMP connector that has the silk screen label shown in the first column.

*Table 2. Signal Re-mapping by Signal Name*

| Silk Screen | Actual Signal |
|---|---|
| CS0_B | CA0_B |
| CS1_B | CA1_B |
| CA0_B | CA2_B |
| CA1_B | CA3_B |
| CA2_B | CA4_B |
| CA3_B | CA5_B |
| CA4_B | CA6_B |
| CA5_B | CA7_B |
| CA6_B | CS0_B |
| PAR_B | CS1_B |
| CB0_B | CB4_B |
| CB1_B | CB5_B |
| CB2_B | CB6_B |
| CB3_B | CB7_B |
| CB4_B | CB0_B |
| CB5_B | CB1_B |
| CB6_B | CB2_B |
| CB7_B | CB3_B |